KING FAHD UNIVERSITY OF PETROLEUM & MINERALS  
*COMPUTER ENGINEERING DEPARTMENT*

COE 405 Design and Modeling of Digital Systems

Term 181 Lecture Breakdown

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| **Lec#** | **Date** | **Topics** | **Ref.** |
| 1 | U 2/9 | Syllabus & Course Introduction. Introduction to Digital Design Methodology. | Chapter 1 |
| 2 | T 4/9 | Digital System Design Cycle, Architecture Design Example. | Chapter 1 |
| 3 | TH 6/9 | Architecture Design Example. Design Space and Evaluation Space, Digital System Complexity. Dealing with Design Complexity, Design Hierarchy, Abstractions, Design Domains & Levels of Abstraction, Design Methods. | Chapter 1 |
| 4 | U 9/9 | Design Methods. Design vs. Synthesis, Synthesis Process, Circuit Synthesis. Hardware Description Languages, Design Automation & CAD Tools. | Chapter 1 |
| 5 | T 11/9 | Definitions: implicant, Prime Implicant, Essential Prime Implicant. Minimum cover, Minimal cover or irredundant cover. Sum of Product (SOP) Simplification Procedure. Shannon's Expansion, Boolean Expansion Based on Orthonormal Basis. | Chapter 2 |
| 6 | TH 13/9 | Boolean Expansion Based on Orthonormal Basis. Don’t Care Conditions. SOP Simplification Procedure using Don’t Cares, Product of Sum (POS) Simplification. | Chapter 2 |
| 7 | U 16/9 | SOP Simplification Procedure using Don’t Cares. Combinational Circuits Design Procedure, Iterative Design. | Chapter 2 |
| 8 | T 18/9 | Iterative Design. Decoders, Implementing Functions using Decoders. Multiplexers, Implementing Functions using Multiplexers. | Chapter 2 |
| 9 | TH 20/9 | **(Quiz#1)** |  |
|  | U 23/9 | **National Day Holiday** |  |
| 10 | T 25/9 | Introduction to Verilog, Why use HDL?, Definition of a Module. Gate-level modeling, Verilog primitives. Verilog Syntax, Verilog Data Types. Module instantiation. | 4.1-4.2 |
| 11 | TH 27/9 | Organization of a Testbench for Verifying a Unit Under Test (UUT), Testbench Template, Propagation Delay, Inertial Delay, Assign Statement, Propagation Delay & Continuous Assignment. Verilog Generate Constructs, Verilog Generate Loop. | 4.2-4.4 |
| 12 | S 29/9 | Conditional If-Generate & Case-Generate. Sequential Circuit Models: Mealy vs. Moore. D-Latch, D-FF, Synchronous vs. Asynchronous Reset, Sequential Circuit Design. | Chapter 3 |
| 13 | U 30/9 | Sequential Circuit Design Examples. State Minimization. | Chapter 3 |
| 14 | T 2/10 | State Minimization: Partition refinement method, implication chart method. | Chapter 3 |
| 15 | TH 4/10 | State encoding. Sequential Circuit Timing, Timing Constraints, FF set up time, Clock to Q delay, FF hold time, Clock Skew. Peak to Peak Jitter. | Chapter 3 |
| 16 | U 7/10 | Hold Time violation, metastability, synchronizing flip-flops. **(Quiz#2)** | Chapter 3 |
| 17 | T 9/10 | Behavioral Modeling, Data Types for Behavioral Modeling, Assign Statement, Verilog Operators, Always Block, Procedural Assignment. | 5.1-5.3 |
| 18 | TH 11/10 | Tutorial on using FPGA Board. |  |
|  | TH 11/10 | **Last Day for Dropping with W** |  |
| 19 | U 14/10 | Wire vs. Reg, Algorithm-Based Models, if statement, Case statement. Behavioral Models of Multiplexor, Encoder, Decoder. D Latch, D Flip-flop (synchronous & asynchronous reset).  Data Flow/ RTL Models: Shifter. Behavioral Models of Multiplexor. | 5.6-5.9 |
| 20 | T 16/10 | Behavioral Models of Multiplexor. Encoder, Decoder. Seven Segment Display Decoder, FSM Modeling, FSM Test Bench. | 5.6-5.11, 5.14 |
| 21 | TH 18/10 | Parallel Load Register.Shift Register, MultiFunction Register, Up-Down Counter, Up-Down Counter: Testbench. **(Quiz#3)** |  |
| 22 | U 21/10 | Data Path & Control Unit Partitioning, Data Path Design, Registers, Shift Registers, Modulo N (i.e. divide by N) Counters. Counters as Clock frequency dividers. Three-State Devices, A Register Bank with a 4-bit Data Bus, Design Steps. Digital System Design Example: Traffic Light Controller. | 5.14-5.15 |
| 23 | T 23/10 | Traffic Light Controller. Algorithmic State Machine (ASM) Chart, Timing in ASM Charts. ASM Chart => Controller, ASM Chart => Architecture/Data Processor, Implementing Controller. | 5.14-5.15 |
| 24 | TH 25/10 | ASM Chart => Controller, ASM Chart => Architecture/Data Processor, Implementing Controller, Algorithmic State Machine and DataPath (ASMD) Chart, ASMD Chart for 4-bit Counter. Design Examples: 2:1 Decimator, One’s Count Circuit. | 5.14-5.15 |
|  | S 27/10 | **Midterm Exam** |  |
| 25 | U 28/10 | Midterm Exam Solution. One’s Count Circuit. Implementation of Data Path and Control Units of One’s Count Circuit. | 5.14-5.15 |
| 26 | T 30/10 | Scores Avg., Max. & Min., Counting Number of Elements ≥Target Value. | 5.14-5.15 |
| 27 | TH 1/11 | Design Examples: Counting Number of Elements ≥Target Value, Election Circuit. | 5.14-5.15 |
| 28 | U 4/11 | Register File & Memory Modeling. Design Examples: Transition Counting Circuit, Average of Serial Scores. | 5.14-5.15 |
| 29 | T 6/11 | Design Examples: A Simple Network DeMux, Sequential Signed Multiplier. |  |
| 30 | TH 8/11 | Design Examples: Sequential Unsigned Divider.Behavioral Modeling of ASM, Linear Feedback Shift Register (LFSR), LFSR Modeling, Repetitive Algorithms: for loop. Adder/Subtracter, Modeling Unsigned Division using for loop. | 5.9-5.11 |
|  | TH 8/11 | **Last Day for Dropping all Courses with W** |  |
| 31 | U 11/11 | Modeling Signed Multiplication using for loop. Repetitive Algorithms: repeat loop, while loop, disable, forever. Tasks and Functions. | 5.11-5.13 |
| 32 | T 13/11 | **(Quiz#4)** |  |
| 33 | TH 15/11 | File I/O system functions and tasks. Programmable Logic and Storage Devices: History of Computational Fabrics. | Chapter 8 |
| 34 | U 18/11 | ASIC vs. FPGA, FPGA Advantages, Reconfigurable Logic, Anti-Fuse-Based Approach. RAM Based Field Programmable Logic, Xilinx FPGA Families, The Xilinx 4000 CLB. LUT Mapping, Configuring the CLB as a RAM, FPGA Interconnect, Basic I/O Block Structure, CLB Structure, 5-Input Functions, Distributed RAM. | Chapter 8 |
| 35 | T 20/11 | Distributed RAM., Shift Register, Carry & Control Logic. Adder Implementation, Carry Chain, 18 x 18 Embedded Multiplier. FPGA Design Flow – Mapping, Placement & Route. Memory Types, FPGA Memory Implementation, LUT-Based RAMS. | Chapter 8 |
| 36 | TH 22/11 | Block RAM. Block RAM Logic Diagram, Block RAM Data Combinations and ADDR Locations, Read & Write Operations, Write Modes, Conflict Avoidance, Using Core Generator. | Chapter 8 |
| 37 | U 25/11 | Using IP Core Generator. **(Quiz#5)** |  |
| 38 | T 27/11 | Using IP Core Generator. Circuit Synthesis, Multilevel logic synthesis, Logic Network modeling. Network Optimization, Area and Delay estimation. | 6.1 |
| 39 | TH 29/11 | Multilevel Logic Transformations: Elimination, Decomposition, Factoring. | 6.1 |
| 40 | U 2/12 | Multilevel Logic Transformations: Extraction, Simplification, Substitution, Fast Extraction. Synthesis & Testability. | 6.1 |
| 41 | T 4/12 | Synthesis & Testability. Timing Issues in Multiple-Level Logic Optimization. Network Delay Modeling, topological critical path, false path, Algorithms for Delay Minimization. | 6.1 |
| 42 | TH 6/12 | Algorithms for Delay Minimization. Behavioral or High-Level Synthesis: CDFG, scheduling, allocation. High-Level Synthesis Examples. Synthesis of Combinational Logic. | 6.1 |
|  | TH 6/12 | **Dropping all Courses with WP/WF** |  |
| 43 | U 9/12 | **(Quiz#6)** |  |
| 44 | T 11/12 | Synthesis of Priority Structures. Exploiting Logical Don’t Care Conditions, Resource Sharing, Synthesis of Sequential Logic with Latches. Synthesis of Three-State Devices and Bus Interfaces, Synthesis of Sequential Logic with Flip-Flops. Synthesis of Explicit State Machine. Exploiting Logical Don’t Care Conditions. Synthesis of Gated Clocks and Clock Enable, Operator Grouping, Expression Substitution, Synthesis of loops. | 6.1-6.6 |
| 45 | TH 13/12 | No Class |  |