Name: Id#

COE 306, Term 161

Introduction to Embedded Systems

Quiz# 3 Solution

 Date: Thursday, Nov. 24, 2016

# **Q1.** A memory device is read by putting a read request on the bus for a single bus cycle using a **R/W'** signal. The memory device then puts the read data on the bus 2 bus cycles after receiving the request. The memory asserts a **Ready** signal to indicate that the data is ready. We would like to read three consecutive 32-bit words at memory addresses 0x10, 0x14 and 0x18. Assume that the data bus is 32-bit wide.

1. Use a timing diagram to show the bus signals required to read the three locations using non-burst requests. Show the bus clock, the address, the read data, and any other required signals.



1. Assuming a fixed burst size of 3, use a timing diagram to show the required bus signals to read the three locations using burst requests. Assume that an active-low burst signal must be asserted for a single cycle only for each burst read request. Assume that each consecutive data in a burst will be ready two cycles after the previous data.

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# **Q2.** A real-time system receives data through an I/O device, the CPU processes the data, then the results of the processing are transferred to system memory. The I/O device, the CPU, and the memory controller are all on the same system bus, which runs at 1MHz. The CPU runs at 10 MHz. Each bus transaction (transfer) between any two devices on the bus takes 4 bus cycles, 1 of which is used to transfer data, and the remaining cycles are used by the bus protocol. The bus has 16 data lines, transferring 16 bits per data-transfer cycle.

# The I/O device receives 256 bytes at a time. While processing the received data, for each received byte, the CPU generates 2 bytes. Only generated data is transferred from the CPU to system memory.

# If the I/O device receives new data at a rate of 500 times per second (256 bytes each), how many CPU cycles can be spent processing each byte without violating the real-time requirements? Assume that the memory is fast enough to handle any requests received by the memory controller.

NI/O = 256 B x 500 = 128000 B/s

 TI/O(N) = (D +O) N/W = 4 x 128000/2= 256000 cycles/s

Nmem = 256 B x 500 x 2 = 256000 B/s

Tmem(N) = 4 x 256000/2 = 512000 cycles/s

Tbus = 256000+ 512000= 768000 cycles/s

tbus = Tbus P = 768000 x 10-6 = 0.768 s

tCPU = 1 - 0.768 = 0.232 s

TCPU = tCPU - fCPU = 0.232 x 10 x 106 = 2320000 cycles/s

Number of CPU cycles can be spent processing each byte without violating the real-time requirements = 2320000 / 128000 = 18.125 => 18 cycles per Byte.