Name:

COE 306, Term 171

Introduction to Embedded Systems Quiz# 3

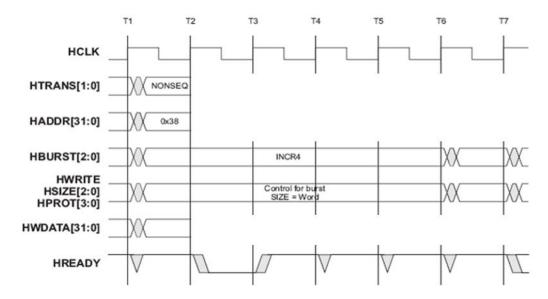
Date: Thursday, Nov. 16, 2017

Q1. Fill in the blank in each of the following questions:

- (1) _______ allows transfers between the CPU and I/O devices without involving the CPU.
- (2) In a microprocessor system, a high speed bus is connected to a low speed bus using

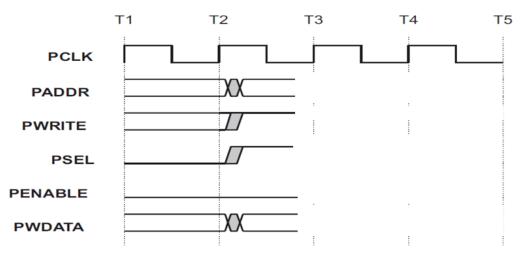
(3) In AMBA, the UART is connected to ______ bus.

(4) In AMBA basic AHB transfer, a slave can insert wait states by



(5) Complete the given timing diagram for an AMBA AHB pipelined burst write transfer:

(6) Complete the given timing diagram for an AMBA APB write transfer:



(7) Given that the match registers are set to have the following values: MR0=100, MR1=421, MR2=78, MR3=53, MR4, 27 and MR5=65. Assume that the timer is configured for PWM mode and that control bits PWMENA2, PWMENA4, PWMENA5, PWMSEL2 and PWMSEL4 are set. Complete the given timing diagram for one PWM cycle:



Q2. A sensor generates 10000 bytes of data every 10ms, and sends them to the CPU over a 2-MHz peripheral bus. The bus is 32-bit wide, and each bus transfer on the bus takes 3 bus cycles, 1 of which is used to transfer data, and the remaining cycles are used by the bus protocol.

i. What is the CPU's time budget (in seconds) for processing each 10000 bytes of sensory data?

ii. If the CPU needs 30 cycles to process each byte of sensory data, what is the lowest frequency at which the CPU can run in order to process the data in time?