KING FAHD UNIVERSITY OF PETROLEUM & MINERALS
COMPUTER ENGINEERING DEPARTMENT

COE 306 Introduction to Embedded Systems

Term 171 Lecture Breakdown

Lec #	Date	Topics	Ref.
1	U17/9	Syllabus and Course Introduction.	
2	T 19/9	What is an Embedded System? Application Examples, Characteristics of Embedded Systems, Implementation Alternatives, Why Use Microprocessors? Platforms. Challenges in Embedded System Design.	1.1-1.2
3	TH 21/9	Challenges in Embedded System Design, Importance of Design Methodology, Embedded System Design Process, Requirements, Specification, Architecture Design. Designing Hardware and Software Components.	1.2-1.3
	U 24/9	**National Day Holiday**	
4	T 26/9	System Integration, Formal System Description: UML. Computer Architecture Taxonomy.	1.3 & 2.1-2.2
5	TH 28/9	RISC vs. CISC, Instruction Set Characteristics. Instruction Execution, ARM Instruction Set, ARM Processor Modes, The ARM Register Set, Program Status Registers, ARM Instruction Set Format, Conditional Execution.	2.2-2.3
6	U 1/10	Conditional Execution, Data Processing Instructions, Arithmetic Operations, Logical Operations, Comparisons, Data Movement.	2.3
7	T 3/10	The Barrel Shifter, Loading 32 bit constants. **(Quiz#1)**	2.3
8	TH 5/10	Loading 32 bit constants. Load / Store Instructions, Pre or Post Indexed Addressing, ARM ADR Pseudo-Op, ARM Branches and Subroutines, Control Flow: If Statement Example, Switch Statement.	2.3
9	S 7/10	For Loop, Examples of Conditional Execution. Examples of Conditional Execution, Block Data Transfer, Stack Operation, Stacks and Subroutines, Function Calls, ARM Procedure Call Standard (APCS). PICmicro.	2.3 & 2.4

10	U 8/10	PICmicro PIC16F Instruction Set, Instruction Memory Organization, Register File Concept, Data Memory Organization, Status Register, Program Counter, Instruction Set Overview. PIC16 Addressing Modes, Register Indirect Addressing Example, Control Flow Instructions. PC Absolute Addressing, PC Relative Addressing, PC Relative Addressing: Lookup Table.	2.4
11	T 10/10	TI C55X Organization, TI C55x Microarchitecture, Instruction Buffer Unit (I Unit), Program Flow Unit (P Unit), Address-Data Flow Unit (A Unit), Data Computation Unit (D Unit), Memory Organization, C55x Addressing Modes, Absolute Addressing, Direct Addressing Modes. C55x Indirect Addressing Modes, C55x Data Instructions Examples, Control Flow Instructions, Loops and Procedure Calls, TI 64X DSP.	2.5-2.6
12	TH 12/10	Input and Output (I/O) Devices, Busy-Wait (Polling) I/O, Interrupt I/O, Interrupt I/O Examples.	3.1-3.2
13	U 15/10	Interrupt I/O Examples, Interrupts vs. Polling I/O, Interrupt Implementation. Supporting Multiple I/O Devices, Interrupt Priorities.	3.2
14	T 17/10	Interrupt Vectors, Interrupt Overhead, Interrupts in ARM7, Supervisor Mode, Exceptions, Traps. Co-Processors, Memory System Overview, Caches, Average memory access time, Multiple Levels of Cache, Cache Organizations & Policies, Virtual Memory.	3.4, 3.5
15	TH 19/10	Virtual Memory, Memory Management Unit Tasks, Segmentation, Paging, The Page Table, Multi-Level Page Tables, MMU in ARM. Virtual Memory System Example.	3.5
16	U 22/10	Multi-Level Page Tables, CPU Performance, CPU Power Consumption, CPU Power-Saving Strategies, Power-Down Costs.	3.5-3.7
17	T 24/10	Computing Platforms, Platform Hardware Components. **(Quiz#2)**	4.1-4.3
18	TH 26/10	Platform Software Components, The CPU bus. Bus Protocols, Timing Diagrams, Read Followed by Write, Reading From A Slow Device, Burst Read, Direct Memory Access (DMA), DMA Controller, System Bus Configurations, ARM Bus.	4.3-4.4
	TH 26/10	**Last Day for Dropping with W**	
	S 28/10	**Major Exam I**	

19	U 29/10	Solution of Major Exam 1. Advanced High-Performance Bus (AHB).	4.3-4.4
20	T 31/10	Advanced High-Performance Bus (AHB), AHB Arbitration, AHB Signals, Overview of AMBA AHB operation, AHB Basic Transfer, AHB Pipelining, AHB Pipelined Burst Transfers.	4.3-4.4
21	TH 2/11	AHB Burst Types, AHB Control Signals, AHB Split Transfers, AHB Bus Master Interface, AHB Bus Slave Interface, AHB Arbiter Interface, AMBA Advanced Peripheral Bus (APB).	4.4
22	U 5/11	AMBA Advanced Peripheral Bus (APB), APB Write Transfer, APB Read Transfer, AHB-APB Bridge, Interfacing APB to AHB: Read, Burst Read and Write Transfers. SDRAM Operation, Memory Controllers, Memory Channels and Banks. Platform Examples, Choosing a Platform, Development Environment.	4.5
23	T 7/11	Platform-Level Performance, Bandwidth as Performance, Bus Bandwidth Modeling, Memory Performance, Bus Performance Bottlenecks. Pulse Width Modulation Definition.	4.7
24	TH 9/11	Pulse Width Modulation Definition, Pulse Width Modulation Types, Generation of PWM, PWM Applications, LPC176x/5x PWM.	
25	U 12/11	LPC176x/5x PWM.	
26	T 14/11	Embedded Software Components, Software State Machine, Seat Belt Controller, An Elevator System Controller.	5.1-5.2
27	TH 16/11	Implementation of An Elevator System Controller, Circular Buffer.	5.1-5.2
28	U 19/11	**(Quiz#3)**	
29	T 21/11	Queues, Array-Based Queue Implementation, Producer/Consumer Systems. Types of Data Transmission: Serial vs. Parallel. Synchronous vs. Asynchronous Transmission.	5.2
30	TH 23/11	Asynch. Transmission: Data Word and Control Bits, Simplex vs Duplex, BAUD & Bit Rates, Serial Peripheral Interface (SPI), SPI Operation, SPI Clock Polarity and Phase, SPI Slave Configurations.	
	TH 23/11	**Last Day for Dropping all Courses with W**	
31	U 26/11	Serial Peripheral Interface (SPI), SPI Operation, SPI Clock Polarity and Phase, SPI	

		Slave Configurations, SPI Applications, SPI Advantages & Disadvantages, LPC176x/5x SPI Interface Implementation.	
32	T 28/11	LPC176x/5x SPI Interface Implementation. Inter-Integrated Circuit (I2C) Bus, I2C Bus Characteristics, I2C Bus Definitions, I2C Electrical Aspects, Bit Transfer on the I2C Bus, Start and Stop Conditions1st Byte in Data Transfer on I2C Bus, Acknowledgements.	
	W 29/11	**Major Exam II**	
33	TH 30/11	I2C Addressing, Acknowledgements, Data Transfer on the I2C Bus, Data Formats. Solution of Major Exam II.	
34	U 3/12	Multi-Master I2C Systems, Arbitration Between Two Masters, I2C Bus Advantages & Disadvantages, Example – EEPROM.	
35	T 5/12	Using mbed and project introduction.	
36	TH 7/12	LPC176x/5x I^2C Interface.	
37	U 10/12	LPC176x/5x I^2C Interface. Universal Asynchronous Receiver Transmitter (UART), Asynchronous Serial Transmission, Asynchronous Serial Reception, UART Error Conditions, DCE and DTE, Normal 9-Wire Serial Cable.	
38	T 12/12	LPC176x/5x UART Interface.	
39	TH 14/12	Processes and Operating Systems, Tasks and Processes, Multi-Rate Systems, Real-Time Systems. Types of Process Timing Requirements, Process Execution Characteristics.	6.1-6.3
40	U 17/12	CPU Utilization, Running Periodic Processes, Real-Time Operating Systems, State of a Process, Preemptive Execution, Context Switching, FREERTOS. The Scheduling Problem, Scheduling Feasibility, Hyperperiod	6.3-6.5
41	T 19/12	Round-Robin Scheduling, Priority-Based Scheduling, Scheduling Metrics, Rate Monotonic Scheduling (RMS). **(Quiz#4)**	6.5
42	TH 21/12	Rate Monotonic Scheduling (RMS), RMS CPU utilization, RMS- Schedulability Check, Earliest-Deadline-First Scheduling, EDFS - Schedulability Analysis, EDFS	6.5
	TH 21/12	**Dropping all Courses with WP/WF**	
43	U 24/12	EDFS – Overload Conditions, FreeRTOS, Task States in FreeRTOS, FreeRTOS Task Functions, Creating Tasks, Running a Periodic Task. Analog-Digital Converter (ADC), A/D	

		Conversion Process, ADC-Error Possibilities: Aliasing, Quantization Error.	
44	T 26/12	Quantization Error & Effective Number of Bits, Conversion Time & Converter Rate, Types of ADC Techniques, Counter or Tracking ADC, Flash ADC.	
45	TH 28/12	Flash ADC, Half-Flash ADC, Successive Approximation ADC, Single Slope Integration ADC, Dual Slope ADC, Delta-Sigma ADC, ADC Types Comparison.	