KING FAHD UNIVERSITY OF PETROLEUM & MINERALS  
*COMPUTER ENGINEERING DEPARTMENT*

COE 306 Introduction to Embedded Systems

Term 161 Lecture Breakdown

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| **Lec#** | **Date** | **Topics** | **Ref.** |
| 1 | U18/9 | Syllabus and Course Introduction. What is an Embedded System? Application Examples, Characteristics of Embedded Systems, Implementation Alternatives, Why Use Microprocessors? | 1.1-1.2 |
| 2 | T 20/9 | What is an Embedded System? Application Examples, Characteristics of Embedded Systems, Implementation Alternatives, Why Use Microprocessors? Platforms. | 1.1-1.2 |
|  | TH 22/9 | National Day Holiday |  |
| 3 | U 25/9 | Challenges in Embedded System Design, Importance of Design Methodology, Embedded System Design Process, Requirements, Specification, Architecture Design. | 1.2-1.3 |
| 4 | T 27/9 | Architecture Design, Designing Hardware and Software Components, System Integration, Formal System Description: UML.  Computer Architecture Taxonomy, RISC vs. CISC, Instruction Set Characteristics. | 1.3 & 2.1-2.2 |
| 5 | TH 29/9 | Instruction Execution, ARM Instruction Set, ARM Processor Modes, The ARM Register Set, Program Status Registers, ARM Instruction Set Format, Conditional Execution, Data Processing Instructions. | 2.2-2.3 |
| 6 | U 2/10 | Data Processing Instructions, Arithmetic Operations, Logical Operations, Comparisons, Data Movement, The Barrel Shifter, Loading 32 bit constants. | 2.3 |
| 7 | T 4/10 | Load / Store Instructions, Pre or Post Indexed Addressing, ARM ADR Pseudo-Op, ARM Branches and Subroutines, Control Flow: If Statement Example, Switch Statement, For Loop, Examples of Conditional Execution. | 2.3 |
| 8 | TH 6/10 | Examples of Conditional Execution, Block Data Transfer, Stack Operation, Stacks and Subroutines, Function Calls, ARM Procedure Call Standard(APCS), Procedure Examples. | 2.3 |
| 9 | U 9/10 | PICmicro PIC16F Instruction Set, Instruction Memory Organization, Register File Concept, Data Memory Organization, Status Register, Program Counter, Instruction Set Overview. | 2.4 |
| 10 | T 11/10 | PIC16 Instruction Set, PIC16 Addressing Modes, Register Indirect Addressing Example, Control Flow Instructions. **(QUIZ#1)** | 2.4 |
| 11 | TH 13/10 | PC Absolute Addressing, PC Relative Addressing, PC Relative Addressing: Lookup Table, TI C55X Organization, TI C55x Microarchitecture, Instruction Buffer Unit (I Unit), Program Flow Unit (P Unit), Address-Data Flow Unit (A Unit), Data Computation Unit (D Unit), Memory Organization, C55x Addressing Modes, Absolute Addressing, Direct Addressing Modes. | 2.4-2.5 |
| 12 | U 16/10 | C55x Indirect Addressing Modes, C55x Data Instructions Examples, Control Flow Instructions, Loops and Procedure Calls, TI 64X DSP. Input and Output (I/O) Devices, Busy-Wait (Polling) I/O | 2.5-2.6, 3.1-3.2 |
| 13 | T 18/10 | Interrupt I/O, Interrupt I/O Examples, Interrupts vs. Polling I/O, Interrupt Implementation. | 3.2 |
| 14 | TH 20/10 | Interrupt Implementation, Supporting Multiple I/O Devices, Interrupt Priorities. **(QUIZ#2)** | 3.2 |
| 15 | U 23/10 | Interrupt Priorities, Interrupt Vectors, Interrupt Overhead, Interrupts in ARM7, Supervisor Mode, Exceptions, Traps | 3.2-3.3 |
| 16 | T 25/10 | Co-Processors, Memory System Overview, Caches, Average memory access time, Multiple Levels of Cache, Cache Organizations & Policies, Virtual Memory. | 3.4, 3.5 |
| 17 | TH 27/10 | Virtual Memory, Memory Management Unit Tasks, Segmentation, Paging, The Page Table, Multi-Level Page Tables, MMU in ARM. Virtual Memory System Example. | 3.5 |
|  | TH 27/10 | **Last Day for Dropping with W** |  |
|  | S 29/10 | **Major Exam I** |  |
| 18 | U 30/10 | CPU Performance. Solution of Major Exam I. | 3.6 |
| 19 | T 1/11 | CPU Power Consumption, CPU Power-Saving Strategies, Power-Down Costs. Computing Platforms, Platform Hardware Components, Platform Software Components, The CPU bus. | 3.7, 4.1-4.3 |
| 20 | TH 3/11 | The CPU bus, Bus Protocols, Timing Diagrams, Read Followed by Write, Reading From A Slow Device, Burst Read, Direct Memory Access (DMA), DMA Controller, System Bus Configurations, ARM Bus, Memory Components, Random-Access Memory. | 4.3-4.4 |
| 21 | U 6/11 | Advanced High-Performance Bus (AHB), AHB Arbitration, AHB Signals, Overview of AMBA AHB operation, AHB Basic Transfer, AHB Pipelining, AHB Pipelined Burst Transfers, AHB Burst Types, AHB Control Signals. | 4.3-4.4 |
| 22 | T 8/11 | AHB Split Transfers, AHB Bus Master Interface, AHB Bus Slave Interface, AHB Arbiter Interface, AMBA Advanced Peripheral Bus (APB), APB Write Transfer, APB Read Transfer, AHB-APB Bridge, Interfacing APB to AHB: Read, Burst Read and Write Transfers. SDRAM Operation, Memory Controllers, Memory Channels and Banks. | 4.4 |
| 23 | TH 10/11 | Platform Examples, Choosing a Platform, Development Environment, Platform-Level Performance, Bandwidth as Performance, Bus Bandwidth Modeling, Memory Performance, Bus Performance Bottlenecks. | 4.5, 4.7 |
|  | 13-17 Nov. | Mid-Term break |  |
| 24 | U 20/11 | Embedded Software Components, Software State Machine, Circular Buffer, Queues. | 5.1-5.2 |
| 25 | T 22/11 | Array-Based Queue Implementation, Producer/Consumer Systems.  Standard Bus Architecture Presentations: CoreConnect, Sonics Smart Interconnect, STBus. | 5.2 |
| 26 | TH 24/11 | Models of Programs, Data Flow Graph, Control-Data Flow Graph. **(QUIZ#3)** | 5.3 |
| 27 | U 27/11 | Compilation and Execution, The Assembler, The Symbol Table, Object File, Linking, The Linker, Example. | 5.4 |
| 28 | T 29/11 | Linking Example, Loaders, Static vs. Dynamic Linking, Linking Considerations: Memory Map, Reentrant Programs. | 5.4 |
| 29 | TH 1/12 | The Compilation Process, Basic Compilation: Expressions, Compiler Optimizations: Register Allocation. | 5.5 |
|  | TH 1/12 | **Last Day for Dropping all Courses with W** |  |
| 30 | U 4/12 | Basic Compilation : Control Structures, Procedures, Data Structures, Compiler Optimizations: Expression Simplification, Dead Code Elimination, Procedure Inlining, Loop Transformations, Loop Tiling, Array Padding. | 5.5 |
| 31 | T 6/15 | **(QUIZ#4)** |  |
| 32 | TH 8/12 | M3pi and mbed (presentation by Saleh Al-Saleh) |  |
|  | S 10/12 | **Major Exam II** |  |
| 33 | U 11/12 | No Class. |  |
| 34 | T 13/12 | Processes and Operating Systems, Tasks and Processes, Multi-Rate Systems, Real-Time Systems. (Solution of Major Exam II). | 6.1-6.3 |
| 35 | TH 15/12 | Types of Process Timing Requirements, Process Execution Characteristics, CPU Utilization, Running Periodic Processes, Real-Time Operating Systems, State of a Process, Preemptive Execution, Context Switching, FREERTOS. | 6.3-6.4 |
| 36 | U 18/12 | The Scheduling Problem, Scheduling Feasibility, Hyperperiod, Round-Robin Scheduling, Priority-Based Scheduling, Scheduling Metrics, Rate Monotonic Scheduling (RMS). | 6.5 |
| 37 | T 20/12 | Rate Monotonic Scheduling (RMS), RMS CPU utilization, RMS- Schedulability Check, Earliest-Deadline-First Scheduling, EDFS - Schedulability Analysis, EDFS – Overload Conditions. | 6.5 |
| 38 | TH 22/12 | Interprocess Communication Mechanisms, Shared Memory Communication, Unix Procedure for Using Shared Memory, Shared Memory, Pros and Cons, Message Passing Communication, Synchronization in Message Passing, IPC Requirements. | 6.6 |
| 39 | U 25/12 | Pipes, Signals, Mailboxes, Sockets. Types of Data Transmission: Serial vs. Parallel. Synchronous vs. Asynchronous Transmission. | 6.6 |
| 40 | T 27/12 | Asynch. Transmission: Data Word and Control Bits, Simplex vs Duplex, BAUD & Bit Rates, Serial Peripheral Interface (SPI), SPI Operation, SPI Clock Polarity and Phase, SPI Slave Configurations, SPI Applications, SPI Advantages & Disadvantages, LPC176x/5x SPI Interface. |  |
| 41 | TH 29/12 | LPC176x/5x SPI Registers, LPC176x/5x SPI Exception Conditions, SPI Master Operation, Inter-Integrated Circuit (I2C) Bus, I2C Bus Characteristics, I2C Bus Definitions, I2C Electrical Aspects, Bit Transfer on the I2C Bus, Start and Stop Conditions1st Byte in Data Transfer on I2C Bus, Acknowledgements. |  |
|  | TH 29/12 | Dropping all Courses with WP/WF |  |
| 42 | U 1/1 | I2C Addressing, Acknowledgements, Data Transfer on the I2C Bus, Data Formats. |  |
| 43 | T 3/1 | Multi-Master I2C Systems, Arbitration Between Two Masters, I2C Bus Advantages & Disadvantages, Example – EEPROM, LPC176x/5x I2C Interface. |  |
| 44 | TH 5/1 | LPC176x/5x I2C Interface. **(QUIZ#5)** |  |
| 45 | U 8/1 | Universal Asynchronous Receiver Transmitter (UART), Asynchronous Serial Transmission, Asynchronous Serial Reception, UART Error Conditions, DCE and DTE, Normal 9-Wire Serial Cable, LPC176x/5x UART Interface. |  |