***King Fahd University of Petroleum and Minerals***

***College of Computer Science and Engineering***

***Computer Engineering Department***

**COE 306: INTRODUCTION TO EMBEDDED SYSTEMS**

**Term 171 (Fall 2017-2018)**

**Final Exam**

**Tuesday Jan. 2, 2018**

**Time: 150 minutes, Total Pages: 11**

**Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ ID:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Section: \_\_\_\_\_\_\_**

**Notes:**

* Do not open the exam book until instructed
* Answer all questions
* All steps must be shown
* Any assumptions made must be clearly stated

|  |  |  |
| --- | --- | --- |
| **Question** | **Max Points** | **Score** |
| **Q1** | **41** |  |
| **Q2** | **19** |  |
| **Q3** | **9** |  |
| **Q4** | **10** |  |
| **Q5** | **11** |  |
| **Total** | **90** |  |

Dr. Aiman El-Maleh

# **[41 Points]**

# **(Q1)** Fill in the blank in each of the following questions:

## The analog to digital conversion process involves the following two main steps \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ and \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## In ADC, aliasing occurs when \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Adding 1 extra bit to an n-bit ADC increases the SNR by \_\_\_\_\_\_\_\_\_\_\_ dB.

## Given an 8-bit ADC with conversion time equal to 100 ns, the maximum frequency that the signal A sin(2πf) can have to guarantee conversion accuracy is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Given an analog signal that has a range from -5v to +5v, the analog value 2.5v will be converted to the following hex value \_\_\_\_\_\_\_\_\_\_\_\_ using 8-bits successive approximation ADC.

## Given an analog signal that has a range from -5v to +5v, complete the table given below showing the generated 8-bits for the analog value 2.5v using delta-sigma modulator:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input | **δ** | **∑** | Out | DAC |
| 2.5 | 2.5 | 2.5 | 1 | +5v |
| 2.5 | -2.5 | 0.0 | 1 | +5v |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |
|  |  |  |  |  |

## The fastest ADC technique is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_, while the ADC technique with highest resolution is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Parallel communication is faster than serial communication for short distances. However, bandwidth of parallel wires is much lower than bandwidth of serial wires for long distances because \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## To double the signal to noise ratio in serial transmission for long distances, \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ are used.

## 

## The advantages of synchronous serial transmission over asynchronous serial transmission are \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ while the disadvantages are \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Given UART with 3 bits of protocol (start, stop and parity), 7 bits of data, 14400 baud rate, and 2 bits per symbol, the information rate is \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Using SPI interface, a single master is connected to two slaves as follows:

## Two advantages of SPI interface are \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ and two disadvantages are \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## In I2C interface, data line can only change state when the clock is \_\_\_\_\_\_\_.

## In I2C interface, when a master is reading multiple bytes from a slave, a master informs the slave that a read byte is the last to be read by sending \_\_\_\_\_\_\_\_\_\_\_\_ signal.

## In I2C interface connecting multiple masters, bus arbitration occurs as follows: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Two advantages of I2C interface are \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ and two disadvantages are \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Using UART, transmitting character 'W'=1010111 with odd parity, 7 data bits and one stop bit, the following data waveform is generated:

## In UART, when the stop bit is 0, this causes \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ error.

## In LPC176x UART 0 interface, given that bit 0 in line state register (LPC\_UART0->LSR) is set when the receiver buffer register (LPC\_UART0->RBR) holds an unused character, the following code is used to receive a character in variable ch:

## \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## In LPC176x UART 0 interface, given that bit 5 in line state register (LPC\_UART0->LSR) is set when the transmitter holding register (LPC\_UART0->THR) is empty, the following code is used to transmit a character in variable ch:

## \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## Real time operating systems solve the main problems of a cooperative multitasking system based on two basic concepts \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_, \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

## In FreeRTOS, a task can be in one of the following states \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_.

**[19 Points]**

# **(Q2)** Assume that the following periodic processes are ready at time 0. We would like to schedule these processes using RMS and EDF scheduling techniques. In each case, compute the schedule for an interval equal to the least-common multiple of the periods of the processes. If processes have the same priority, schedule processes to minimize preemption. If processes have the same priority under all these criteria then give priority in the following order P1, P2, P3.

|  |  |  |
| --- | --- | --- |
| **Process** | **Execution Time** | **Period (Deadline)** |
| P1 | 1.0 | 3 |
| P2 | 1.0 | 4 |
| P3 | 2.0 | 6 |

1. **(2 points)** Compute CPU utilization.
2. **(3 points)** Compute the response time for P3 under RMS. Is there a feasible schedule under RMS? Justify your answer.
3. **(5 points)** Schedule the processes using an RMS policy. If a schedule does not meet the required deadlines for all processes, complete the schedule and indicate this in your solution.
4. **(5 points)** Schedule the processes using an EDF policy. If a schedule does not meet the required deadlines for all processes, complete the schedule and indicate this in your solution.
5. **(4 points)** Is it possible to find a feasible schedule where all deadlines for all processes are met using both RMS and EDF if the execution time of P1 is increased to 1.25? Justify your answer.

**[9 Points]**

# **(Q3)** Three periodic tasks T1, T2 and T3 are to be executed on a system with task periods 50ms for T1, 200ms for T2 and 1s for T3.

1. **(6 marks)** It is required to execute the three tasks using a single timer that is configured to expire every 50ms Write a timer interrupt handler (ISR) in C that runs the three tasks according to their periods using a single counter. Assume that each task is run by calling a function of its name, e.g. T1().
2. **(3 marks)** Briefly explain how such three periodic tasks could execute using FreeRTOS.

**[10 Points]**

**(Q4)** Given 24WC32 EEPROM that is 400 KHz I2C Bus Compatible. The EEPROM is 32KBit memory organised as 4K x 8bit with 12 address bits. The EEPROM device address is 1010111. It supports byte write and page write with a 32-byte write buffer. It also supports immediate/current address reading, selective/random read, and sequential read. Use S and P to indicate a start and stop conditions on the data line.

1. **(2 points)** Show the block diagram interface of the microcontroller with the 24WC32 EEPROM using I2C Bus.
2. **(4 points)** Show the data waveform for writing a single data byte to a selected address.
3. **(4 points)** Show the data waveform for reading a single data byte from a specified address location.

**[11 Points]**

**(Q5)** Given an analog signal in the range of 0v to +5v, it is required to convert the analog signal value **4.6v** into a digital signal with 4-bit resolution.

1. **(3 points)** Show the 4-bit converted signal using Flash ADC. Clearly explain your answer.
2. **(4 points)** Show the 4-bit converted signal using Half-Flash ADC with each Flash ADC generating two bits. Clearly explain your answer.
3. **(4 points)** Show the 4-bit converted signal using Successive Approximation ADC. Clearly explain your answer.

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