COE 306, Term 161

Introduction to Embedded Systems

Assignment# 3 Solution
Due date: Sunday, Nov. 20, 2016

Q.1. Assume an A/D converter is supplying samples at 44.1 kHz.
  (a) How much time is available per sample for CPU operations?

   Time per sample = 1 / 44.1 k = 0.0227 ms

  (b) If the interrupt handler executes 100 instructions obtaining the sample and passing it
     to the application routine, what is the CPU utilization of a 20 MHz RISC processor
     that executes 1 instruction per cycle?

   CPU can execute (20 * 1000000) instructions in one second.

   Each sample needs 100 instructions.

   In one second, 44100 * 100 = 4410000 instructions need to be executed for the
   samples.

   CPU utilization = 4410000/(20000000) = 22.05%.

Q.2. A memory device is read by putting a read request on the bus for a single bus cycle using
     a **R/W'** signal. The memory device then puts the read data on the bus 2 bus cycles after
     receiving the request. The memory asserts a **Ready** signal to indicate that the data is ready.
     We would like to read two consecutive 32-bit words at memory addresses 0x1000 and
     0x1004. Assume that the data bus is 32-bit wide.

  (a) Use a timing diagram to show the bus signals required to read the two locations using
     non-burst requests. Show the bus clock, the address, the read data, and any other
     required signals.
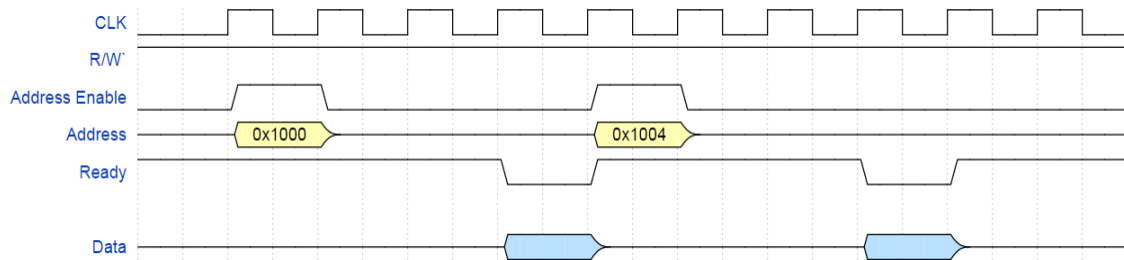
(b) Assuming a fixed burst size of 2, use a timing diagram to show the required bus signals to read the two locations using burst requests. Assume that an active-low burst signal must be asserted for a single cycle only for each burst read request. Assume that each consecutive data in a burst will be ready two cycles after the previous data.
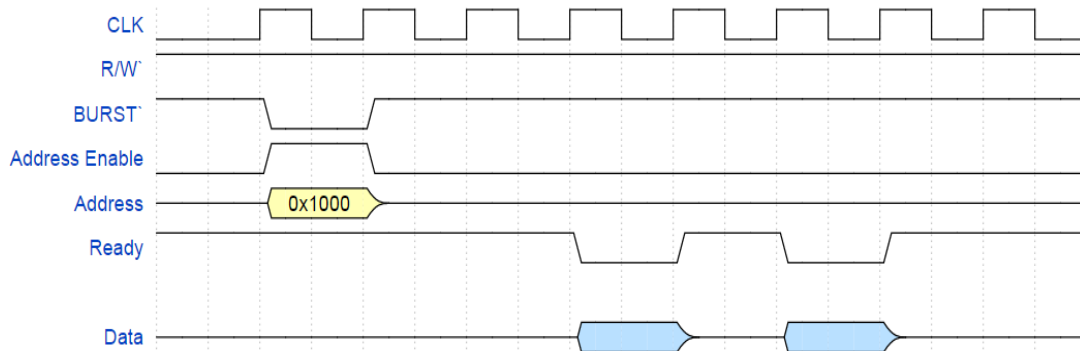
Q.3. We would like to investigate the performance of a bus system in relation to a digital audio application. Digital audio is specified by three main parameters:

1. Number of channels, e.g. stereo audio uses two channels.

2. Sampling rate: number of digital samples per second.

3. Sample size (or bit depth): number of bits per sample.

Assume a system bus that runs at 1.5 MHz, and requires a total of 6 cycles to complete a single 16-bit transfer. Assuming uncompressed 6-channel audio (5.1 speaker configuration), what is the best combination of sampling rate and sample size that can be handled by this system bus? Justify your choice.
Typical sampling rates: 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz (Audio CD), 48 kHz (DVD).
Typical sample sizes: 8-bit, 16-bit (Audio CD), 20-bit, 24-bit, 32-bit.

First, we find the number of bits that the described system bus can transfer per second, N_{bus}:

$$T = (D + O)\frac{N}{W} \implies Nbus = \frac{WT}{(D + O)} = \frac{1.5 \times 10^6 \times 16}{6} = 4 \times 10^6 \; bits$$

Considering Audio CD quality (sampling rate: 44.1 kHz, sample size: 16 bits), the required bandwidth is:
$N_{audio} = 6 \times 44,100 \times 16 = 4,233,600$ bit/second $> 4 \times 10^6$

We can either reduce the sampling rate, or the sample size, to lower the required bandwidth to match the system bus capacity:

$N_{audio1} = 6 \times 32,000 \times 16 = 3,072,000$ bit/second $< 4 \times 10^6$

$N_{audio2} = 6 \times 44,100 \times 8 = 2,116,800$ bit/second $< 4 \times 10^6$

Since Naudio2 halves the sample size, it is expected to have a greater impact on audio quality. Hence, reducing the sampling rate is preferred, resulting in a sampling rate of 32 kHz and a sample size of 16 bits.

Furthermore, we can achieve better audio quality by increasing the sample size of Naudio1 from 16 to 20 bits:
N_{audio3} = 6 x 32,000 x 20 = 3,840,000 bit/second < 4 x 10^6

Therefore, the best combination that the system can handle is 32,000 sampling rate and 20 bit samples.

Q.4. A real-time system receives data through an I/O device, the CPU processes the data, then the results of the processing are transferred to system memory. The I/O device, the CPU, and the memory controller are all on the same system bus, which runs at 1MHz. The CPU runs at 10 MHz. Each bus transaction (transfer) between any two devices on the bus takes 5 bus cycles, 1 of which is used to transfer data, and the remaining cycles are used by the bus protocol. The bus has 32 data lines, transferring 32 bits per data-transfer cycle.

The I/O device receives 512 bytes at a time. While processing the received data, for each received byte, the CPU generates 4 bytes. Only generated data is transferred from the CPU to system memory.

If the I/O device receives new data at a rate of 200 times per second (512 bytes each), how many CPU cycles can be spent processing each byte without violating the real-time requirements? Assume that the memory is fast enough to handle any requests received by the memory controller.

$N_{I/O}$ = 512 B x 200 = 102400 B/s

$T_{I/O}(N)$ = (D +O) N/W = 5 x 102400/4= 128000 cycles/s

N_{mem} = 512 B x 200 x 4 = 409600 B/s

$T_{mem}(N)$ = 5 x 409600/4 = 512000 cycles/s

T_{bus} = 128000+ 512000= 640000 cycles/s

t_{bus} = T_{bus} P = 640000 x 10^{-6} = 0.64 s

t_{CPU} = 1 - 0.64 = 0.36 s

T_{CPU} = t_{CPU} - f_{CPU} = 0.36 x 10 x 10^6 = 3600000 cycles/s

Number of CPU cycles can be spent processing each byte without violating the real-time requirements = 3600000 / 102400 = 35.156 => 35 cycles per Byte.