

COE 306, Term 161

Introduction to Embedded Systems

Assignment# 3

Due date: Sunday, Nov. 20, 2016

- Q.1.** Assume an A/D converter is supplying samples at 44.1 kHz.
- How much time is available per sample for CPU operations?
 - If the interrupt handler executes 100 instructions obtaining the sample and passing it to the application routine, what is the CPU utilization of a 20 MHz RISC processor that executes 1 instruction per cycle?
- Q.2.** A memory device is read by putting a read request on the bus for a single bus cycle using a **R/W'** signal. The memory device then puts the read data on the bus 2 bus cycles after receiving the request. The memory asserts a **Ready** signal to indicate that the data is ready. We would like to read two consecutive 32-bit words at memory addresses 0x1000 and 0x1004. Assume that the data bus is 32-bit wide.
- Use a timing diagram to show the bus signals required to read the two locations using non-burst requests. Show the bus clock, the address, the read data, and any other required signals.
 - Assuming a fixed burst size of 2, use a timing diagram to show the required bus signals to read the two locations using burst requests. Assume that an active-low burst signal must be asserted for a single cycle only for each burst read request. Assume that each consecutive data in a burst will be ready two cycles after the previous data.
- Q.3.** We would like to investigate the performance of a bus system in relation to a digital audio application. Digital audio is specified by three main parameters:
- Number of channels, e.g. stereo audio uses two channels.
 - Sampling rate: number of digital samples per second.
 - Sample size (or bit depth): number of bits per sample.

Assume that a system bus that runs at 1.5 MHz, and requires a total of 6 cycles to complete a single 16-bit transfer. Assuming uncompressed 6-channel audio (5.1 speaker configuration), what is the best combination of sampling rate and sample size that can be handled by this system bus? Justify your choice.

Typical sampling rates: 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz (Audio CD), 48 kHz (DVD).
Typical sample sizes: 8-bit, 16-bit (Audio CD), 20-bit, 24-bit, 32-bit.

- Q.4.** A real-time system receives data through an I/O device, the CPU processes the data, then the results of the processing are transferred to system memory. The I/O device, the CPU, and the memory controller are all on the same system bus, which runs at 1MHz. The CPU runs at 10 MHz. Each bus transaction (transfer) between any two devices on the bus takes

5 bus cycles, 1 of which is used to transfer data, and the remaining cycles are used by the bus protocol. The bus has 32 data lines, transferring 32 bits per data-transfer cycle.

The I/O device receives 512 bytes at a time. While processing the received data, for each received byte, the CPU generates 4 bytes. Only generated data is transferred from the CPU to system memory.

If the I/O device receives new data at a rate of 200 times per second (512 bytes each), how many CPU cycles can be spent processing each byte without violating the real-time requirements?

Assume that the memory is fast enough to handle any requests received by the memory controller.