Name: KEY **Id#**

COE 202, Term 102
Fundamentals of Computer Engineering

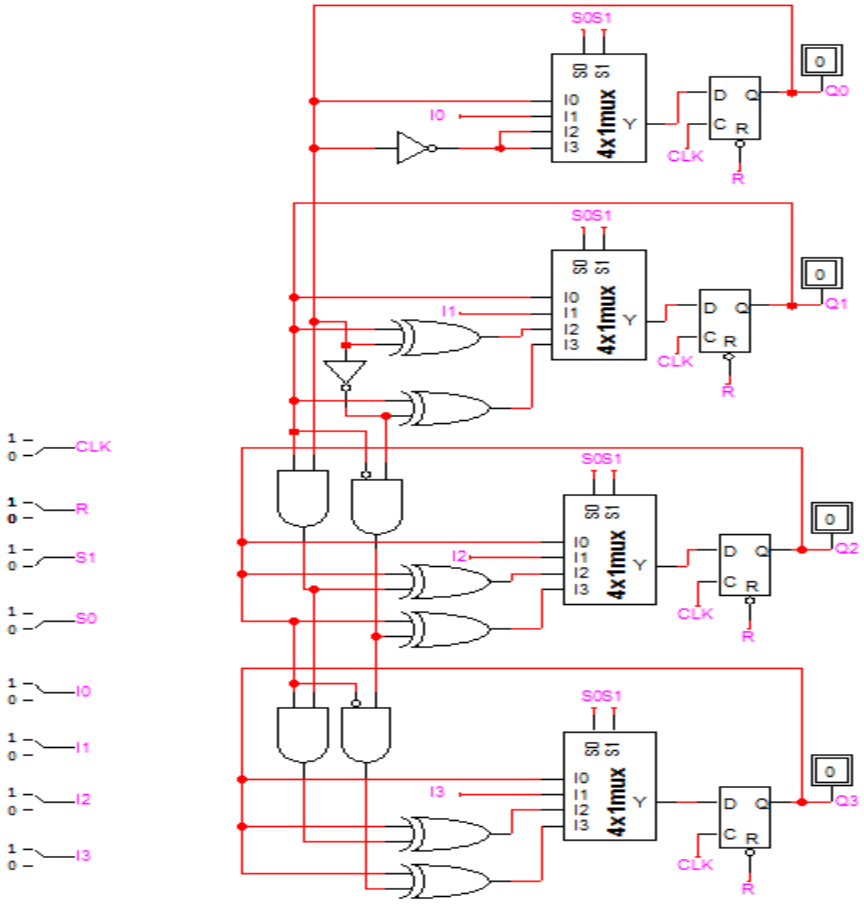
Quiz# 9 (Take Home)

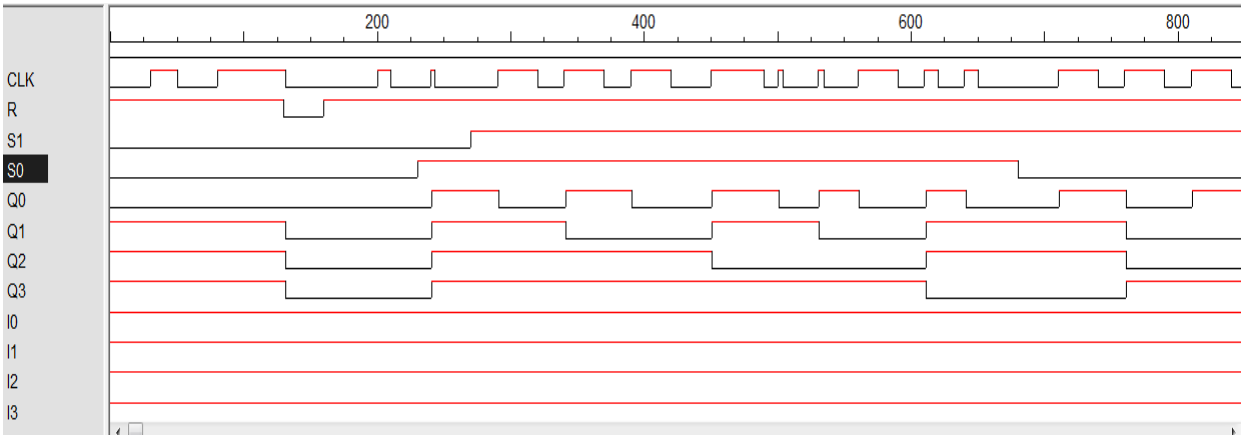
Due date: Sunday, May 29, 2011

Q.1. Design a 4-bit synchronous counter that works based on the following two select inputs:

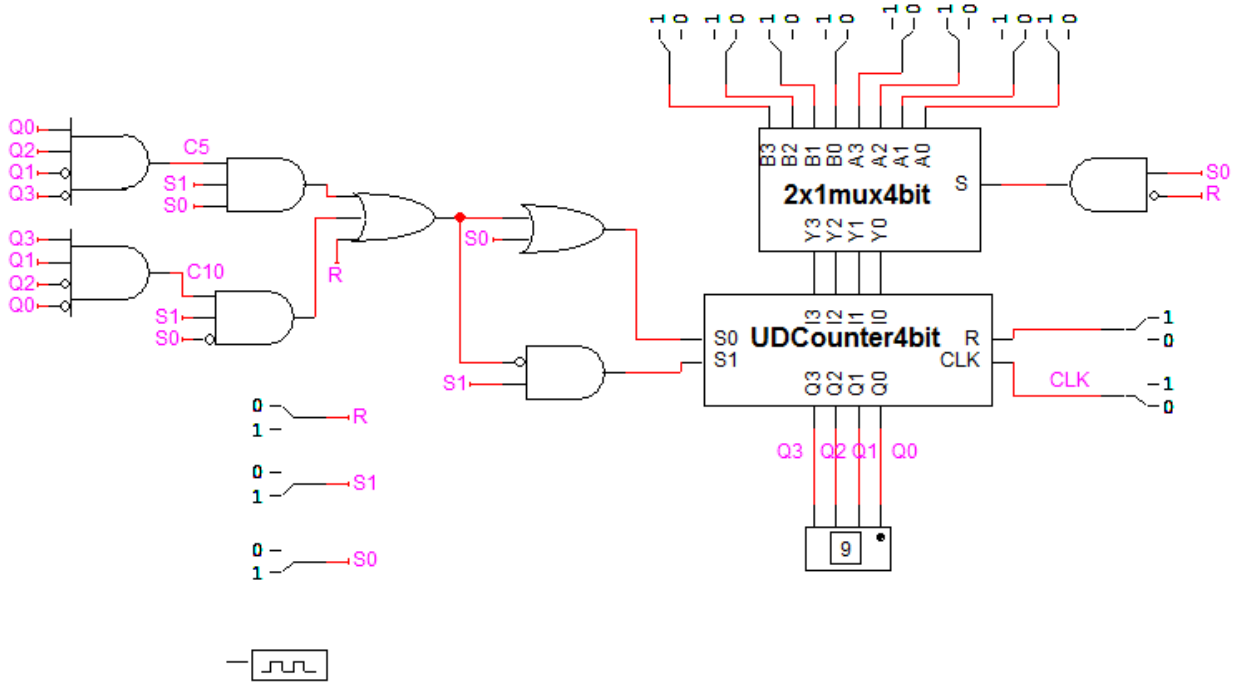
S1	S0	Behavior
0	0	No counting
0	1	Parallel Load the counter
1	0	Count Up
1	1	Count Down

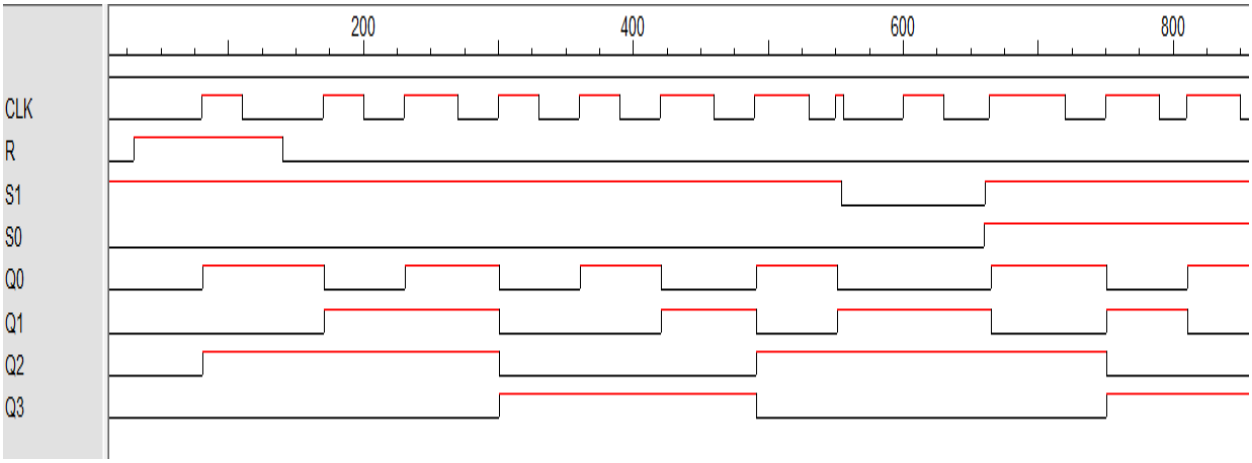
Assume that the counter has asynchronous reset. Model the counter using logic works and verify its correct operation.





Q.2. Use the counter you designed in (Q.1) to count up or down through the following sequence: {5, 6, 7, 8, 9, 10}. When the counter is reset it should start at the value 5 and then the counter should either count up or down. If the counter is counting up and it reaches the value 10 it should back to the value 5. If the counter is counting down and it reaches the value 5, it should go to 10. Model the counter using logic works and verify its correct operation.




200
400
600
800
CLK
R
S1
S0
Q0
Q1
Q2
Q3