Name: KEY **Id#**

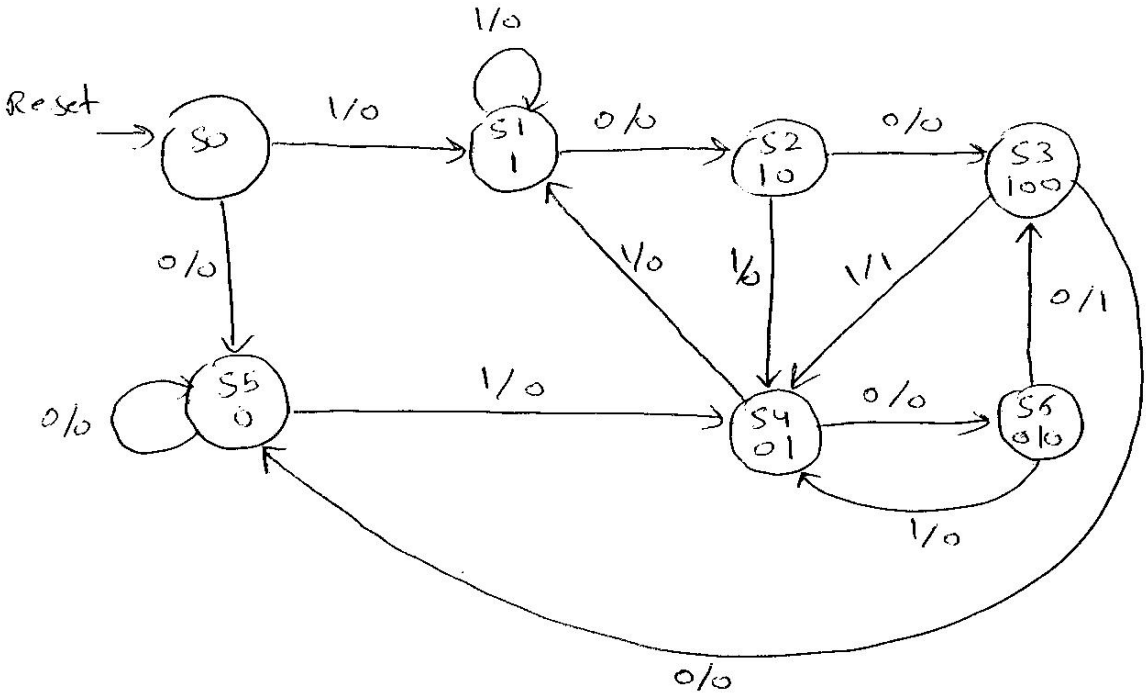
COE 202, Term 102
Fundamentals of Computer Engineering

Quiz# 7 (Take Home)

Due date: Saturday, May 21, 2011

Q.1. It is required to design a sequential circuit that receives a serial input X and produces a serial output Z. The output Z will be 1 when the circuit detects either the sequence 1001 or the sequence 0100 assuming overlapping sequence detection. Derive the state diagram for your circuit, and then obtain the circuit implementation optimizing the output and next state equations assuming D-FFs. Assume the existence of a reset input to reset the machine to a reset state. Model the circuit using logic works and verify its correctness by simulation.

State Diagram:



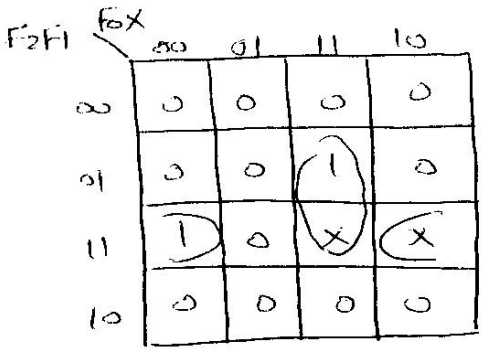
State Table:

Current State	X	Next State	Z
S0	0	S5	0
S0	1	S1	0
S1	0	S2	0
S1	1	S1	0
S2	0	S3	0
S2	1	S4	0
S3	0	S5	0
S3	1	S4	1
S4	0	S6	0
S4	1	S1	0
S5	0	S5	0
S5	1	S4	0
S6	0	S3	1
S6	1	S4	0

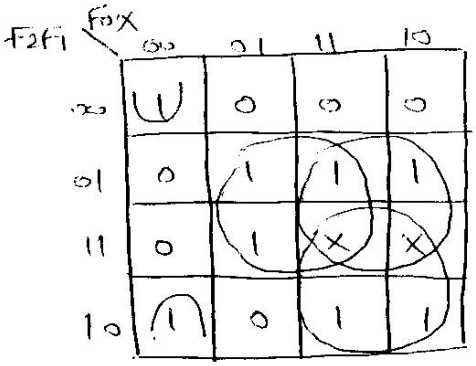
We assign the binary codes to the states and the state table becomes as follows:

Current State F2F1F0	X	Next State F2F1F0	Z
000	0	101	0
000	1	001	0
001	0	010	0
001	1	001	0
010	0	011	0
010	1	100	0
011	0	101	0
011	1	100	1
100	0	110	0
100	1	001	0
101	0	101	0
101	1	100	0
110	0	011	1
110	1	100	0

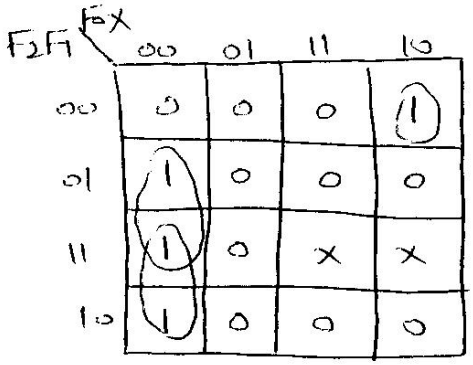
K-map Simplification:



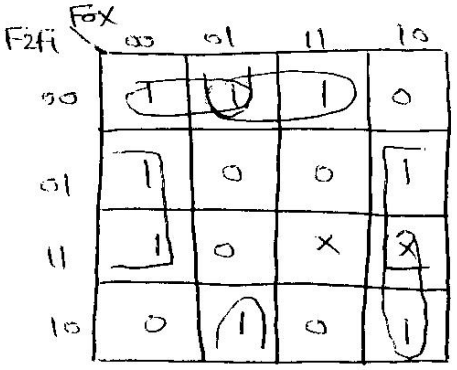
$Z = F_1 F_0 X + F_2 F_1 \bar{X}$



$F_2^+ = \bar{F_1}\bar{F_0}\bar{X} + F_1 F_0 + F_1 X + F_2 F_0$

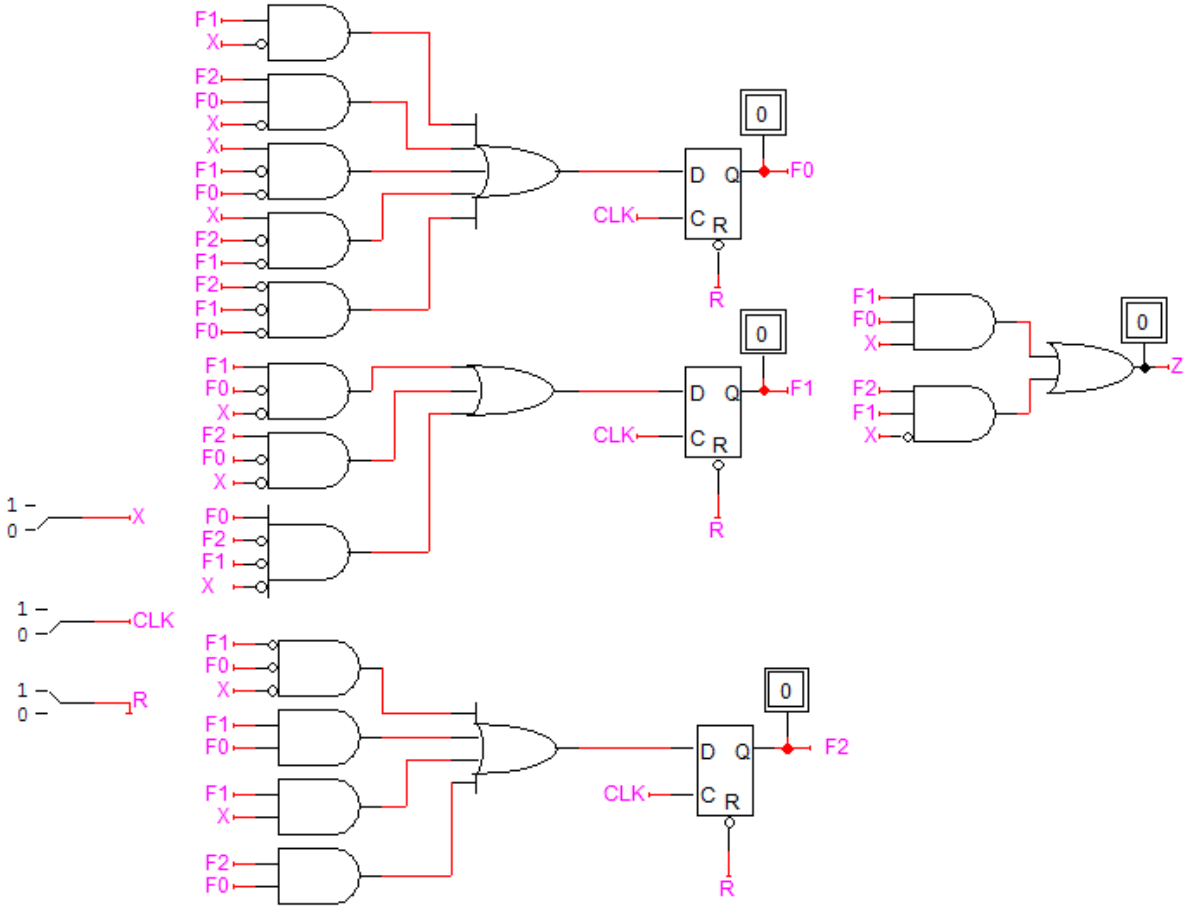


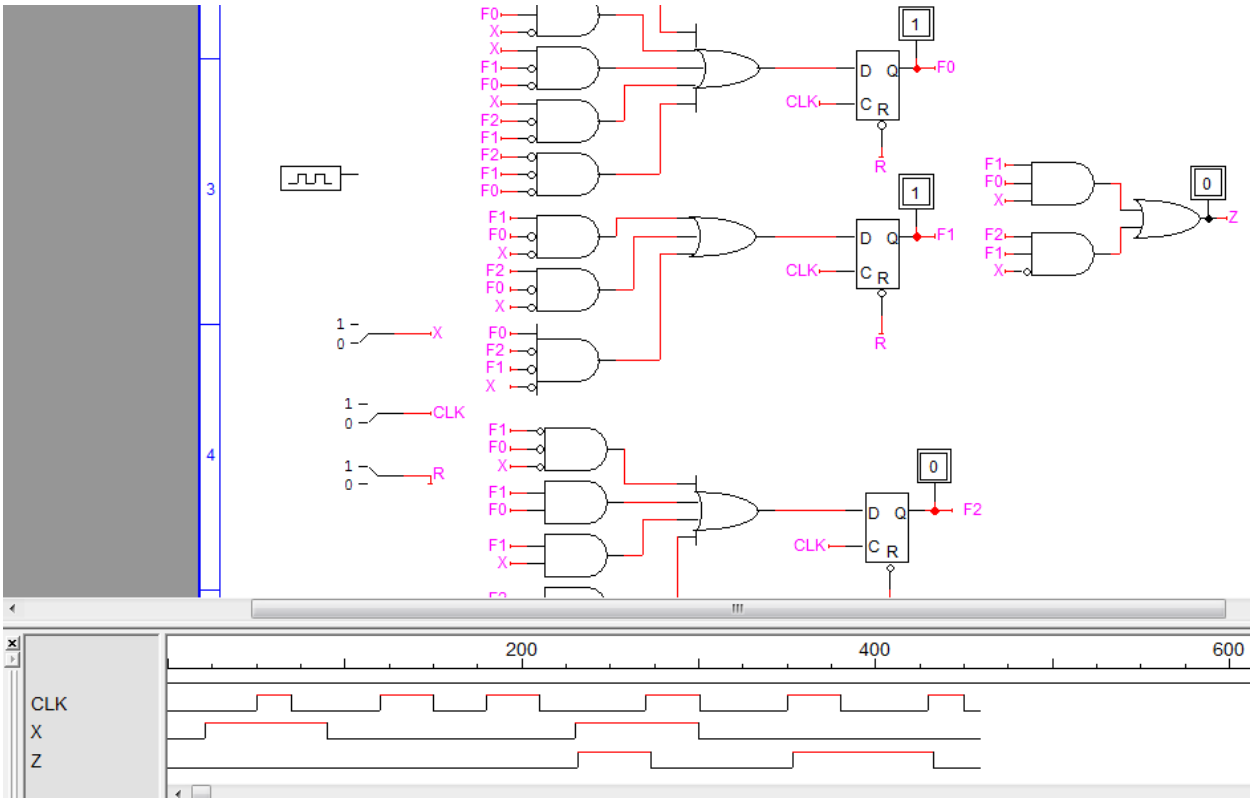
$F_1^+ = F_1 \bar{F_0} \bar{X} + F_2 \bar{F_0} \bar{X} + \bar{F_2} \bar{F_1} F_0 \bar{X}$



$F_0^+ = F_1 \bar{X} + F_2 F_0 \bar{X} + \bar{F_1} \bar{F_0} X + \bar{F_2} \bar{F_1} X + \bar{F_2} \bar{F_1} \bar{F_0}$

Logic Works Circuit:




3
4
F0
X
F1
F2
CLK
R
F1
F2
Z
1
0

200
400
600
CLK
X
Z