Name: **Id#**

COE 202, Term 102
Fundamentals of Computer Engineering

Quiz# 7 (Take Home)

Due date: Saturday, May 21, 2011

Q.1. It is required to design a sequential circuit that receives a serial input X and produces a serial output Z. The output Z will be 1 when the circuit detects either the sequence 1001 or the sequence 0100 assuming overlapping sequence detection. Derive the state diagram for your circuit, and then obtain the circuit implementation optimizing the output and next state equations assuming D-FFs. Assume the existence of a reset input to reset the machine to a reset state. Model the circuit using logic works and verify its correctness by simulation.

Submit your solution as a word document along with the circuits in one zipped file.