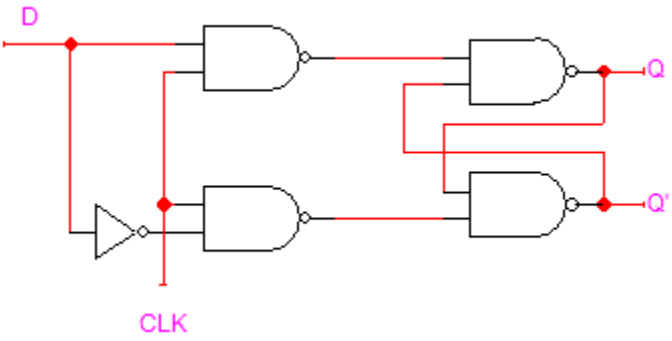
Name: KEY **Id#**

COE 202, Term 102
Fundamentals of Computer Engineering

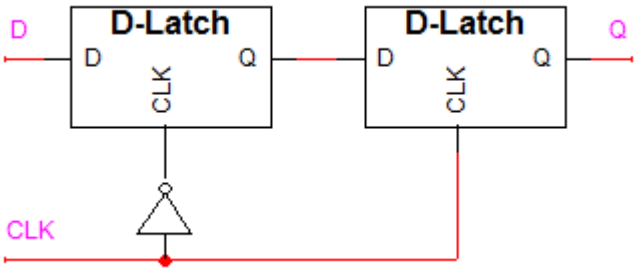
Quiz# 6

Due date: Saturday, May 14, 2011

Q.1. Show the design of a **clocked D-latch** using only Nand gates and inverters.



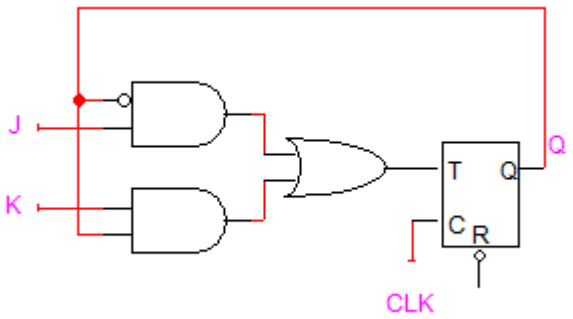
Q.2. Show the design of a **rising-edge triggered D-flip flop** using master-slave D-latches.



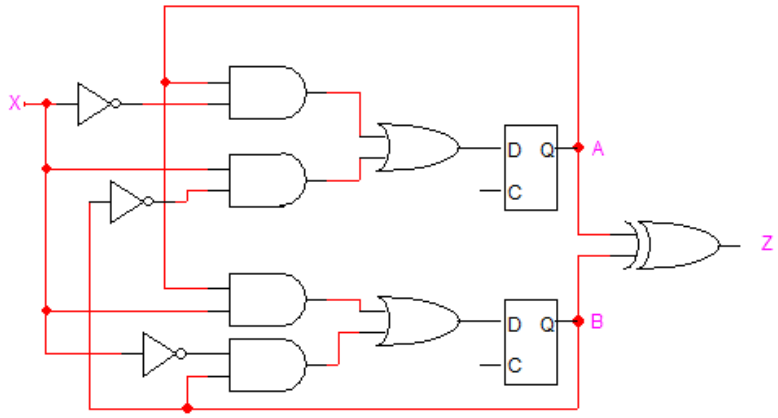
Q.3. Design a rising-edge triggered **JK flip flop** using a rising-edge triggered T flip flop.

Q	J	K	Q+	T
0	0	0	**0**	0
0	0	1	**0**	0
0	1	0	**1**	1
0	1	1	**1**	1
1	0	0	**1**	0
1	0	1	**0**	1
1	1	0	**1**	0
1	1	1	**0**	1

T = Q' J + Q K



Q.4. Derive the **state diagram** of the following sequential circuit with input X and output Z. Determine whether the machine is Mealy or Moore.



The machine is Moore machine as the output depends only on the current state and does not depend on the input. The next state and output equations are as follows:

$D_A = Q_A X' + Q_B' X$
$DB = Q_A X + Q_B X'$
$Z = Q_A \oplus Q_B$

The state diagram is as follows: