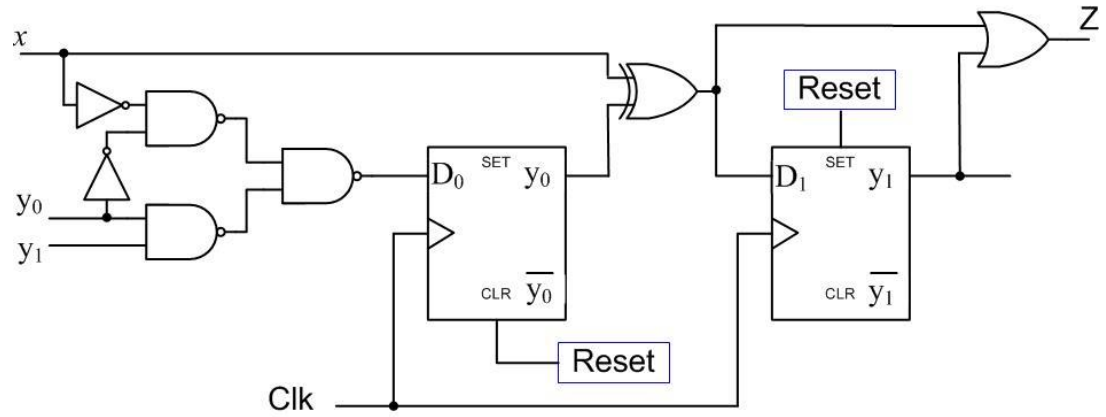
Name: **Id#**

COE 202, Term 141
Digital Logic Design

Quiz# 6

Date: Thursday, Dec. 25

Q1 The sequential circuit shown below has a single output Z, an input *x* together with a Reset input to initialize the circuit. Note that the used D-FFs have direct/asynchronous Clear and Set inputs (shown in the figure as CLR and SET).



a. Is the circuit type Mealy or Moore? Why? (2 point)

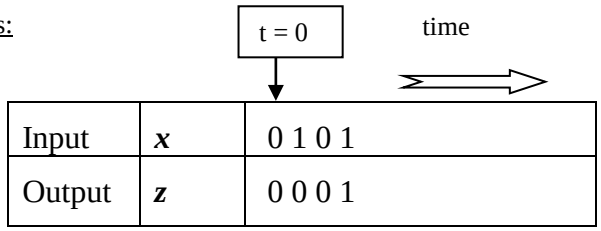
b. Derive expressions for the D_0 and D_1 flip flop inputs and the external output Z. (3 points)

c. Derive the state transition table of the circuit. (4 points)

d. What is the circuit initial state? (1 points)

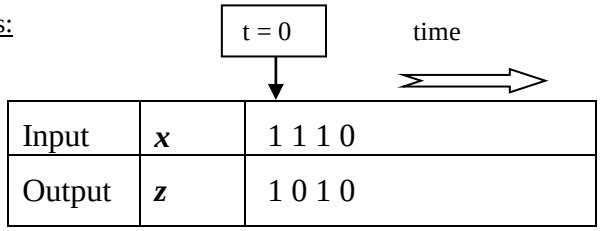
Q2 It is required to design a synchronous sequential circuit that receives a serial inputs **x** and produces a serial output **z** that computes the equation **z=x-2**. Draw the state diagram of this circuit assuming a **Mealy** model. Assume the existence of an asynchronous reset input to reset the machine to a reset state. Two samples of input/output data are given below.
(**NOTE**: You are *only* required to draw the state diagram **Nothing MORE**) (6 points)

Examples:



Input	***x***	0 1 0 1
Output	***z***	0 0 0 1

Examples:



Input	***x***	1 1 1 0
Output	***z***	1 0 1 0