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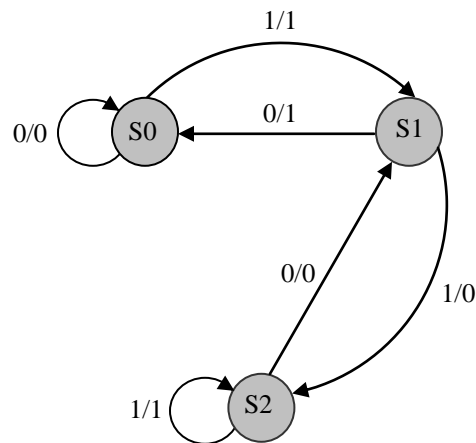
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COE 202, Term 112
Digital Logic Design

Quiz# 6

Date: Monday, May 7

Q1. It is required to design a sequential circuit that receives a serial input X , and produces a serial output Z , equivalent to $3 \cdot X$, i.e., $Z = 3 \cdot X$. The state diagram for this circuit is shown below:



- (i) Show the state table of the sequential circuit.
- (ii) Implement the sequential circuit using D-FFs and the smallest number of gates possible assuming the state assignment: $S0=00$, $S1=01$, and $S2=10$. Minimize your equations using K-map method.
- (iii) Draw the circuit diagram.

Q2. It is required to design a sequential circuit that receives a serial input X and produces a serial output Z . The output Z will be 1 when the circuit detects the sequence 10010 assuming overlapping sequence detection.

- (i) Derive the state diagram for your circuit assuming Mealy model.
- (ii) Derive the state diagram for your circuit assuming Moore model.