Name: **Id#**

COE 202, Term 102
Fundamentals of Computer Engineering

Quiz# 6

Due date: Saturday, May 14, 2011

Q.1. Show the design of a **clocked D-latch** using only Nand gates and inverters.

Q.2. Show the design of a **rising-edge triggered D-flip flop** using master-slave D-latches.

Q.3. Design a rising-edge triggered **JK flip flop** using a rising-edge triggered T flip flop.

Q.4. Derive the **state diagram** of the following sequential circuit with input X and output Z. Determine whether the machine is Mealy or Moore.