Name: Id#

COE 202, Term 201

Digital Logic Design

Quiz# 5 Solution

 Date: Sunday, Nov. 8, 2020

**Question 1: (9 points)**

Given an n-bit signed 2's complement number, **X**,it is required to design an iterative combinational circuit to compute the 2's complement of **X**.

1. Sow the inputs and outputs of the 1-bit 2's complement iterative cell to be used for designing the n-bit 2's complement circuit. (2 Points)
2. Show the truth table of the 1-bit 2's complement cell. (4 Points)
3. Obtain simplified equations for the outputs of the 1-bit 2's complement cell using only the following gate types: NOT, AND, OR, XOR. (2 Points)
4. Using the 1-bit 2's complement cell, draw a block diagram for a circuit to compute the 2's complement of a 3-bit number X. (1 Point)

We will us a signal (One) that propagates between cells to indicate whether we have got one or not.

1-bit

2's comp.

Onei-1

Onei

Xi

Yi

|  |  |  |  |
| --- | --- | --- | --- |
| **Onei-1** | **Xi** | **Onei** | **Yi** |
| **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **1** |
| **1** | **0** | **1** | **1** |
| **1** | **1** | **1** | **0** |

**Yi = Xi ⊕ Onei-1 Onei = Onei-1 + Xi**

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**Alternative Solution:**

We will us a signal (Cin) that propagates between cells to indicate whether we have carry or not. The 2's complement will be computed as the 1's complement + 1.

1-bit

2's comp.

Ci-1

Xi

Ci

Yi

|  |  |  |  |
| --- | --- | --- | --- |
| **Ci-1** | **Xi** | **Ci** | **Yi** |
| **0** | **0** | **0** | **1** |
| **0** | **1** | **0** | **0** |
| **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** |

**Yi = (Xi ⊕ Ci-1)' Ci = Ci-1 Xi'**

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**Question 2. (14 Points)**

1. Fill in all blank cells in the two tables below.

|  |  |
| --- | --- |
| Binary | Equivalent decimal value with the binary interpreted as: |
| Unsigned number | Signed-magnitude number | Signed-1’s complement number  | Signed-2’s complement number |
| 1011 1010 |  186 | -58 | -69 | -70 |

|  |  |
| --- | --- |
| Decimal | Binary representation in 8 bits: |
| Signed-magnitude representation | Signed-1’s complement representation  | Signed-2’s complement representation |
| + 90 | 0101 1010 | 0101 1010 | 0101 1010 |
|  - 90 | 1101 1010 | 1010 0101 | 1010 0110 |

1. Show how the following arithmetic operations are performed using 5-bit signed 2’s-complement system. Check for overflow and mark clearly any overflow occurrences.

|  |  |
| --- | --- |
| (i) 01101 (+13)- 11100 (-4) 01101 (+13)+ 00100 (+4) ------------- 10001 (-15)Overflow: **Yes**/No |  (ii) 10010 (-14)+ 11110 (-2)   10000 (-16)Overflow: Yes/**No** |
| (iii) 11111 (-1)+ 11111 (-1) 11110 (-2) Overflow: Yes/**No** |  (iv) 01011 (+11)- 11011 (-5) 01011 (+11)+ 00101 (+5) ------------- 10000 (-16)Overflow: **Yes**/No |