Name: KEY Id#

COE 202, Term 151

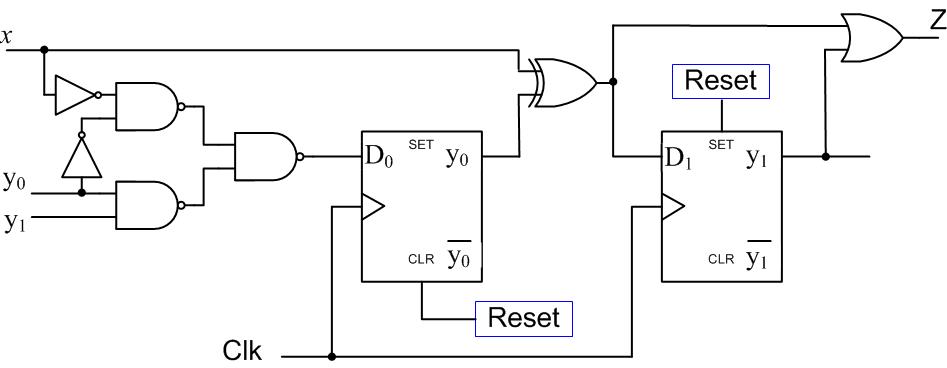
Digital Logic Design

Quiz# 5

Date: Thursday, Dec. 10

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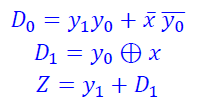
**Q1**. The sequential circuit shown below has a single output Z, an input *x* together with a Reset input to initialize the circuit. Note that the used D-FFs have direct/asynchronous Clear and Set inputs (shown in the figure as CLR and SET).



1. Is the circuit type Mealy or Moore? Why?

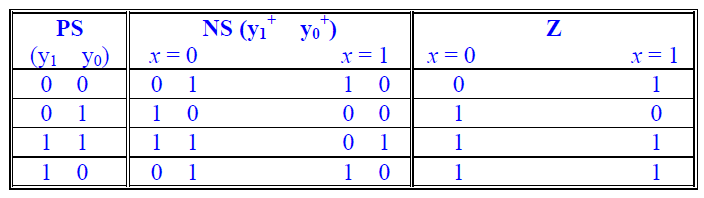
Mealy since Z depends on the input *x*.Mealy since Z depends on the input *x*.

1. Derive expressions for the D0 and D1 flip flop inputs and the external output Z.



1. Derive the state transition table of the circuit.

|  |  |  |
| --- | --- | --- |
| **PS** | **NS (y1+ y0+)** | **Z** |
| (y1 y0) | *x* = 0  *x* = 1 | *x* = 0  *x* = 1 |
| 0 0 | 0 1 1 0 | 1 0 |
| 0 1 | 1 0 0 0 | 0 0 |
| 1 1 | 1 1 0 1 | 1 1 |
| 1 0 | 0 1 1 0 | 1 1 |



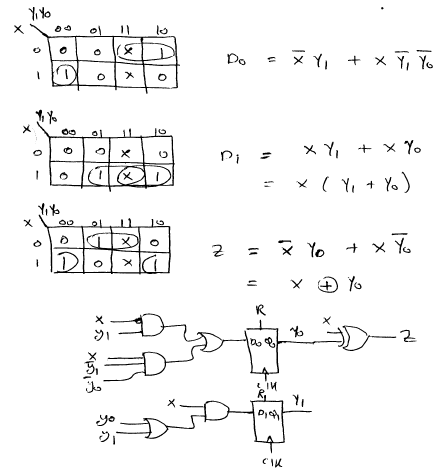
1. What is the circuit initial state?

y1y0=10

**Q2**. Consider the following state transition table for a synchronous sequential circuit that multiplies a binary number by 3 i.e. Z=3\*X. The circuit has a single input **X**, a single output **Z**, and two state variables **Y0**, and **Y1**. The states are encoded using binary codes **00**, **01**, **10.**

|  |  |  |
| --- | --- | --- |
| **PS** (**Y1 Y0**)t | **NS (Y1 Y0)t+1** | **Z** |
| **X = 0 X = 1** | **X = 0 X = 1** |
| 0 0 | 0 0 0 1 | 0 1 |
| 0 1 | 0 0 1 0 | 1 0 |
| 1 0 | 0 1 1 0 | 0 1 |

## Using D-FFs and minimal combinational logic, determine the equations for the D-FF inputs and the output Z for this circuit and draw the resulting circuit. State 00 is the reset state.



# **Q3**. It is required to design a synchronous sequential circuit that receives a serial sequence of **3-bit codes** through input **X** and produces **1** through output **Y** when the received 3-bit code equals either 010 or 110 (i.e., either 0 followed by 1 followed by 0, or 1 followed by 1 followed by 0). Assume the availability of an asynchronous reset input to reset the machine to a reset state. Draw the state diagram of the circuit assuming a **Mealy** model with **minimum** number of states. *You are not required to derive the equations and the circuit*. The following is an example of an input and output sequence:

Example:

**Time**

|  |  |  |
| --- | --- | --- |
| Input | **X** | 0 1 0 0 0 1 0 0 1 1 0 1 1 1 0 |
| Output | **Y** | 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 |

