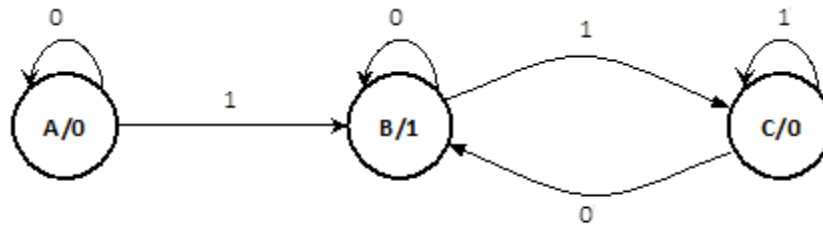


COE 202, Term 142  
Digital Logic Design

Quiz# 5

Date: Tuesday, May 5, 2015

**Q1** The figure below shows a state diagram of a sequential circuit with one input  $x$  and one output  $y$ . Trace the state transitions of this circuit by determining the output and the next state given the sequence of inputs and an initial state as shown in the tables. Assume that the circuit is reset at state A.



(a)

|       |   |   |   |   |   |   |   |   |
|-------|---|---|---|---|---|---|---|---|
| State | A | A | B | B | B | C | B | C |
| $x$   | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| $y$   | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |

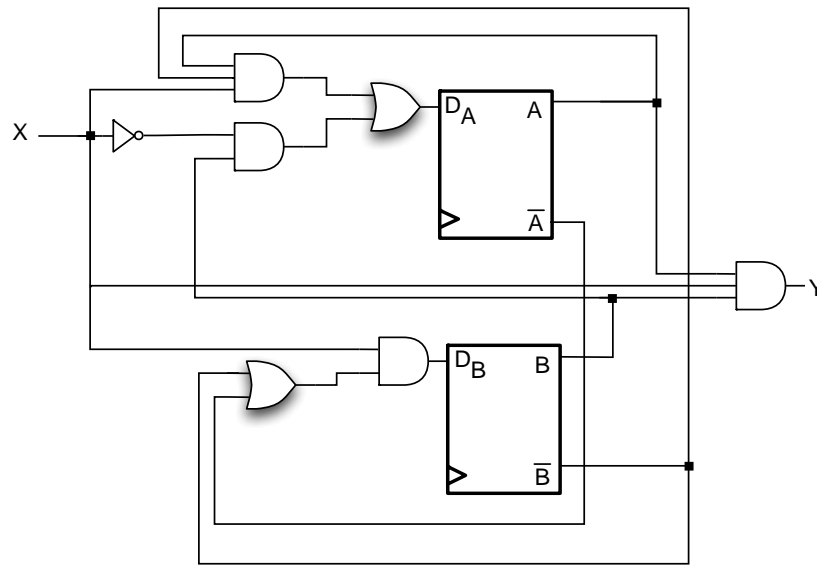
(b)

|       |   |   |   |   |   |   |   |   |
|-------|---|---|---|---|---|---|---|---|
| State | A | B | B | C | C | C | B | C |
| $x$   | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| $y$   | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

(c) What is the operation that the above circuit performs on the input  $x$ ? Choose the correct answer:

- i. Multiplication by 2
- ii. Even parity generation
- iii. Odd parity generation
- iv. **2's complement**

**Q2** Consider the sequential circuit below, which has the input X, the output Y and the two D flip-flops A and B.



(a) Is the circuit type Mealy or Moore?

**Mealy**

(b) Derive logic expressions for the  $D_A$  and  $D_B$  inputs of the flip-flops and the external output Y.

$$D_A = XAB' + X'B$$

$$D_B = X(A'+B')$$

$$Y = XAB$$

(c) Provide a state table showing {present state and external inputs} and {next state and external output}.

| Present State |   | Input | Next state     |                | Output |
|---------------|---|-------|----------------|----------------|--------|
| A             | B | X     | A <sup>+</sup> | B <sup>+</sup> | Y      |
| 0             | 0 | 0     | 0              | 0              | 0      |
| 0             | 0 | 1     | 0              | 1              | 0      |
| 0             | 1 | 0     | 1              | 0              | 0      |
| 0             | 1 | 1     | 0              | 1              | 0      |
| 1             | 0 | 0     | 0              | 0              | 0      |
| 1             | 0 | 1     | 1              | 1              | 0      |
| 1             | 1 | 0     | 1              | 0              | 0      |
| 1             | 1 | 1     | 0              | 0              | 1      |

(d) Derive a complete state diagram for the given circuit.

