Name: KEY Id#

COE 202, Term 141

Digital Logic Design

Quiz# 5

Date: Thursday, Nov. 27

# **Q1** a. Fill in all blank cells in the two tables below.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Binary | Equivalent decimal value with the binary interpreted as: | | | | |
| Unsigned number | Signed-magnitude number | Signed-1’s complement number | Signed-2’s complement number | BCD number |
| 10000000 | 128 | -0 | -127 | -128 | 80 |

|  |  |  |  |
| --- | --- | --- | --- |
| Decimal | Binary representation in 8 bits: | | |
| Signed-magnitude notation | Signed-1’s complement notation | Signed-2’s complement notation |
| - 75 | 11001011 | 10110100 | 10110101 |

b. Using 2’s-complement signed arithmetic in 5 bits, do the following operations **in binary**. Show all your work, and:

- Verify that you get the expected decimal results.

- Check for overflow and mark clearly any overflow occurrences.

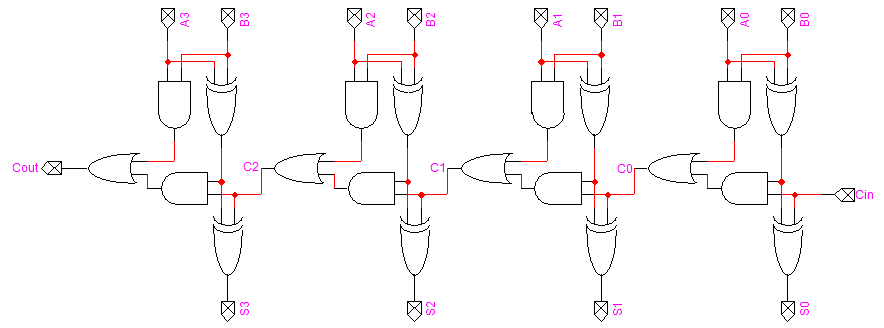
|  |  |
| --- | --- |
| (i)  00111 (+7)  - 10101 (-11)  00111 (+7)  + 01011 (+11)  10010 (-14)  Overflow, we added two positive numbers and we got negative result. | (ii)  10110 (-10)  - 10011 (-13)    10110 (-10)  + 01101 (+13)  00011 (+3)  No overflow. |

c. Consider the signed 2’s complement arithmetic operation A - B in 6 bits. With B = 101100, the largest value allowed for A in order to avoid the occurrence of overflow is (01011)2.

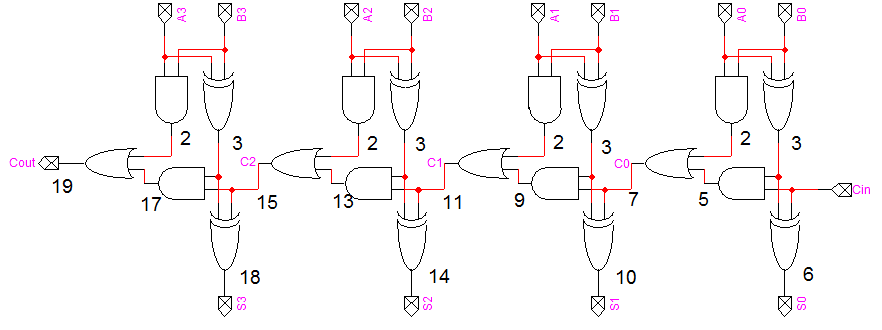
1. B = A + 2’s comp. B = A + 01100 = A + 20. The largest positive value without overflow is +31. Thus A+20=31 => A=11

**Q2** Assume that the delay of a 2-input XOR gate is 3ns while the delay of other gates is equal to the gate’s number of inputs, i.e. the delay of an inverter is 1ns, the delay of a 2-input AND gate is 2ns, the delay of a 2-input OR is 2ns, the delay of a 3-input AND gate is 3ns, the delay of a 3-input OR gate is 3ns, etc.

1. **(6 points)** A 4-bit **Ripple Carry Adder** (RCA) is given below:

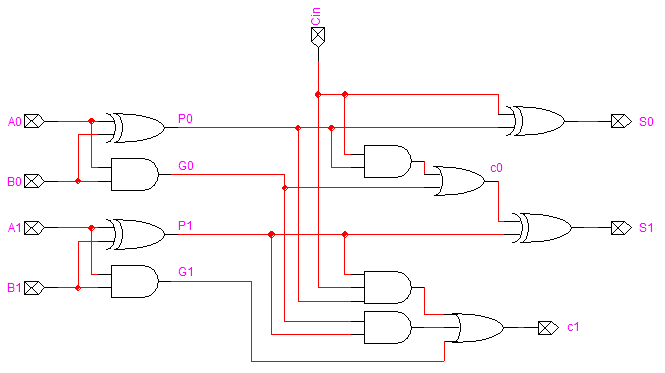


Determine and compute the **longest delay** in the **4-bit Ripple Carry Adder** (RCA).

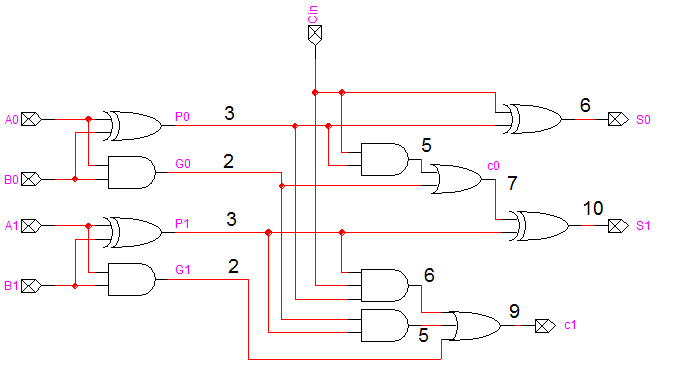


The longest delay is **19 ns** which is along the path from {A0 B0} across the propagate XOR gate until the Cout signal.

1. **(4 points)** Show the design of a **2-bit Carry Look-Ahead Adder** (CLA) by drawing its logic diagram.



1. **(3 points)** Using the delay assumptions given in the beginning of the question, determine and compute the **longest delay** in the **2-bit Carry Look-Ahead Adder** (CLA).



The longest delay is **10 ns** which is along the path from {A0 B0} across the propagate XOR gate until the S1 signal.