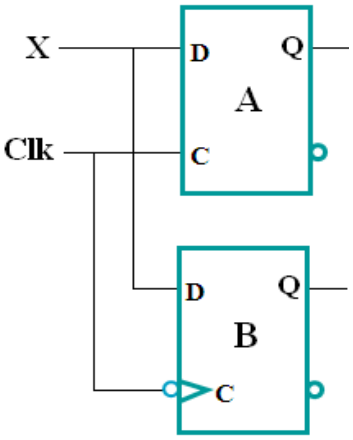
Name: KEY **Id#**

COE 202, Term 132
Digital Logic Design
Quiz# 5

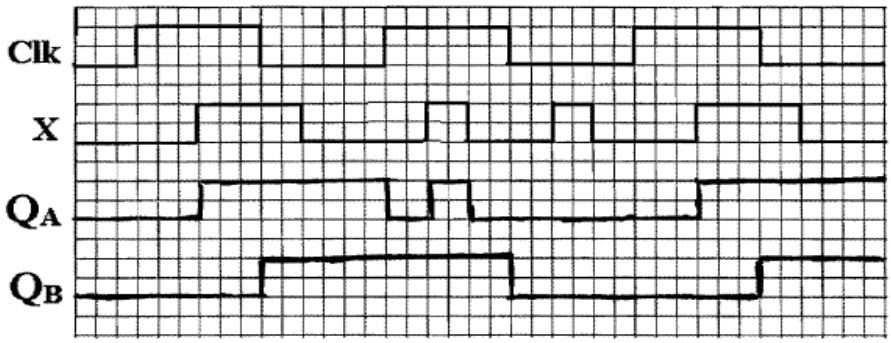
Date: Tuesday, May 6

Question 1. **(13 points)**

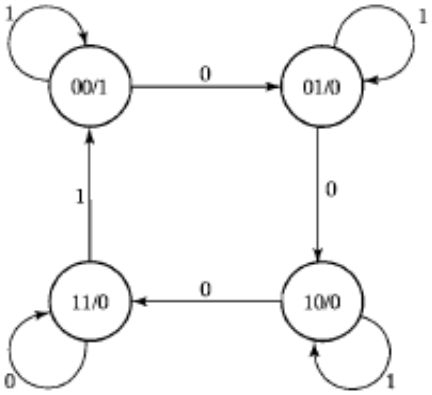
a. In the circuit shown, A is a D-type latch and B is a D-type flip flop. For the input waveforms given for the clock signal (Clk) and the input X, accurately draw the resulting waveforms at outputs $\mathbf{Q_A}$ and $\mathbf{Q_B}$.



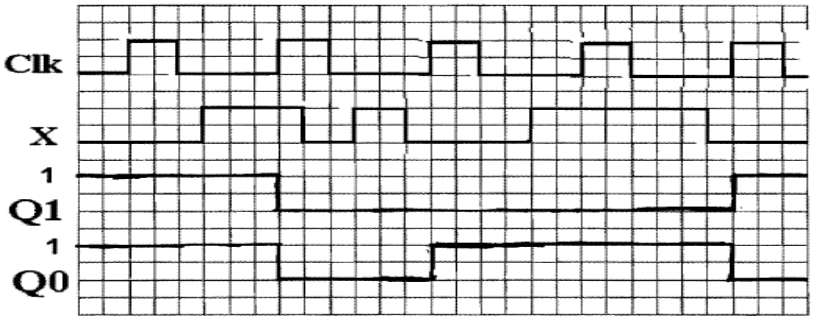
Assume that both Q_A and Q_B are initially at 0.



b. The state diagram shown is for a sequential circuit that has a single input X and a single output Y. The circuit uses two positive edge triggered D-type flip flops Q1 and Q0.



i. Starting with the circuit in state Q1Q0=11, complete the missing waveforms in the timing diagram below.



ii. Let the circuit be in state 00 with input X held permanently at 0. The circuit will end up being stuck at state 11. This state transition requires a minimum time duration of 1.5 ms.

3 x T = 3 x 0.5 ms

Question 2. **(12 Points)**

Consider the sequential circuit opposite and then answer the following questions:

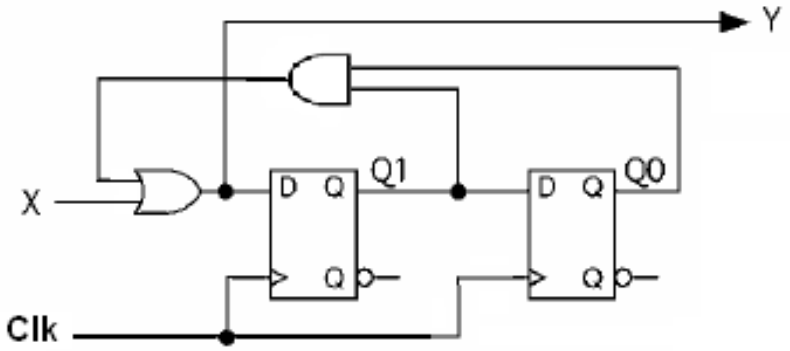
a. Is the circuit Mealy or Moore?
Mealy

b. Provide logical expressions for the flip flop D inputs and the external output

$D_{Q_0} = Q_1$

$D_{Q_1} = Q_0 Q_1 + X$

$Y = Q_0 Q_1 + X$



c. Give both the **state table** and the **state diagram**. Use the layout given below for the state diagram. Note: Q0 represents the LSB of the binary value of the state.

Q_1	Q_0	X	Q_1^+	Q_0^+	Y
0	0	0	0	0	0
0	0	1	1	0	1
0	1	0	0	0	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	1	1