

Name: KEY

Id#

COE 202, Term 131
Digital Logic Design

Quiz# 5

Date: Thursday, Nov. 28

Q1. Fill in all blank cells in the two tables below. All binary representations use 7 bits

Binary	Equivalent decimal value with the binary interpreted as:			
	Unsigned number	Signed-magnitude number	Signed-1's complement number	Signed-2's complement number
1011010	90	-26	-37	-38

Decimal	Binary representation in:		
	Signed-magnitude notation	Signed-1's complement notation	Signed-2's complement notation
-59	1111011	1000100	1000101

b. Using 2's-complement signed arithmetic in **5 bits**, perform the following operations in binary. Show all your work. Verify that you get the expected decimal results.

Check for overflow and mark clearly any occurrences of it.

<p>(i)</p> $\begin{array}{r} 11010 \\ + 11001 \\ \hline 10011 \end{array}$ <p>-6 $+ -7$ -13</p> <p>$= -01101 = -13 \checkmark$ No overflow</p>	<p>(ii)</p> $\begin{array}{r} 00101 \\ - 10100 \\ \hline 00101 \\ + 01100 \\ \hline 01001 \end{array}$ <p>$+5$ -12 $+17 > +15 \rightarrow$ overflow expected</p> <p>$c_n \oplus c_{n-1} = 1$ \therefore overflow</p>
<p>(iii)</p> $\begin{array}{r} (+5) \quad 00101 \\ + (-9) \quad + 10111 \\ \hline -4 \quad 01000 \end{array}$ <p>$= -00100$ $= -4 \checkmark$ No overflow</p>	<p>(iv)</p> $\begin{array}{r} (-6) \quad 11010 \\ - (+8) \quad - 01000 \\ \hline -14 \quad 11010 \\ + 11000 \\ \hline 10010 \end{array}$ <p>$= -01110$ $= -14 \checkmark$ No overflow</p>

c. When doing signed 2's complement arithmetic in **6 bits**, the smallest binary number that will cause overflow when subtracted from 101000_2 is 001001_2

$$\begin{aligned} & \downarrow \\ & = -011000 \\ & = -24 \end{aligned}$$

$$\begin{aligned} \therefore -24 - x &= -33 \\ x &= -24 + 33 = +9 \\ &= 001001 \end{aligned}$$

Q2.

- (a) You are given **one 3-to-8 decoder**, **one NOR gate** and **one OR gate** to implement the two functions given below.

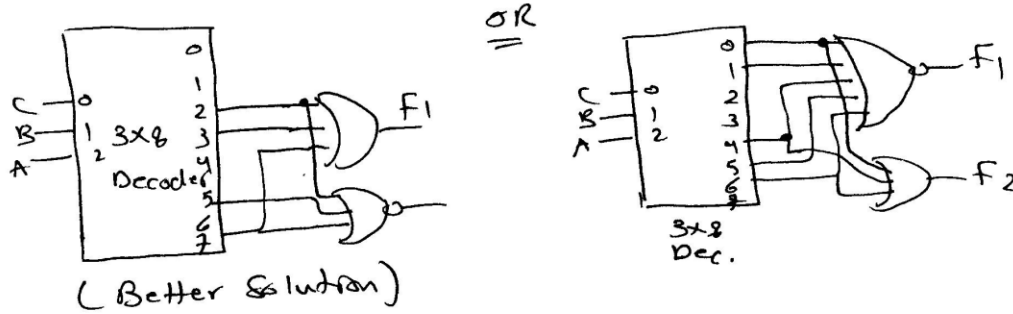
$$F_1(A,B,C) = \prod M(0, 1, 4, 5, 6)$$

$$F_2(A,B,C) = \sum m(0, 4, 6) + \sum d(1, 3)$$

$$F_1 = \sum m(2, 3, 7)$$

$$F_2 = \prod M(2, 5, 7)$$

Draw the circuit and properly label all input and output lines.



- (b) Given the truth table below for a function with four inputs (A, B, C and D) and one output F, implement F using a 4-to-1 MUX (with 2 select lines) and additional logic. Show how you obtained your solution, and properly label all input and output lines. Apply A and B to the select inputs.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

} F = D

} F = 1

} F = \bar{C}

} F = 0

