Name: KEY **Id#**

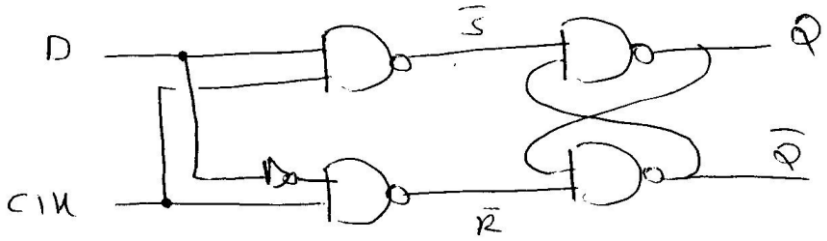
COE 202, Term 122
Digital Logic Design

Quiz# 5

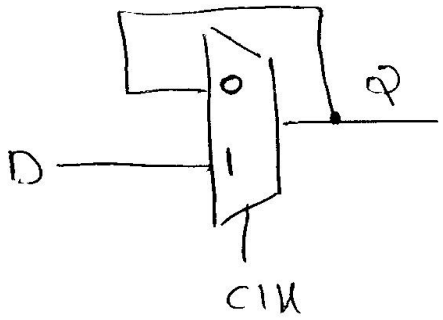
Date: Monday, April 29

Q1.

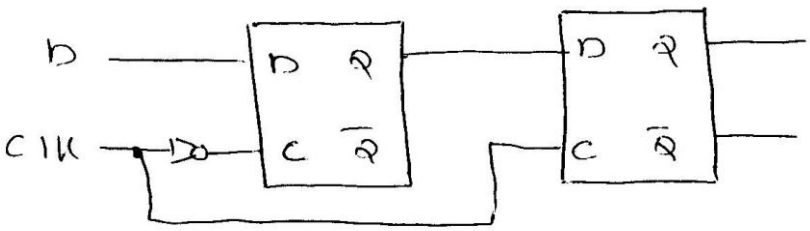
(i) Design a D-Latch using only NAND gates and inverters.



(ii) Design a D-Latch using only a 2x1 Multiplexer.



(iii) Design a **<u>rising-edge</u>** triggered D flip flop using only D-Latches and inverters.

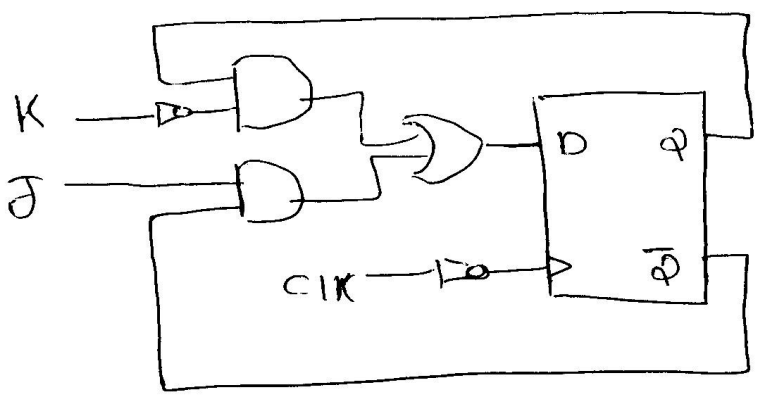


Q2. Design a **falling-edge** triggered JK flip flop using a **rising-edge** triggered D flip flop. Show the design steps.

Q	J	K	Q^+	D
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	0	0

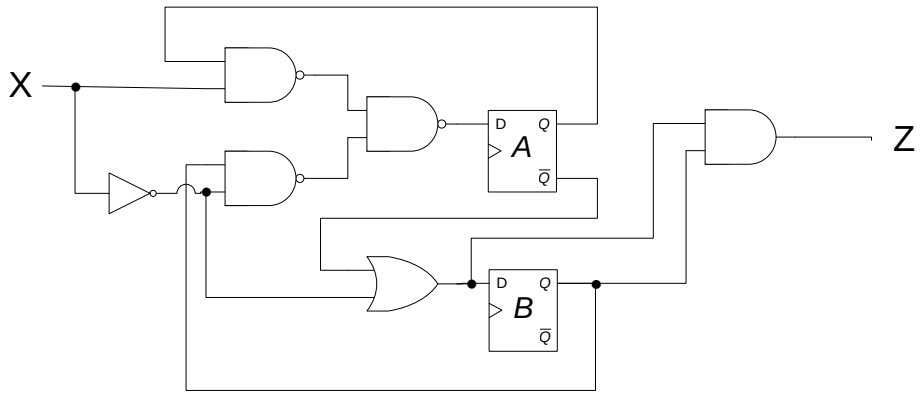
Q \ JK	00	01	11	10
0	0	0	1	1
1	D	0	0	1

$$D = J\bar{Q} + \bar{K}Q$$



Q3.

(i) Derive the state table and state diagram for the following circuit with a single input X, and a single output Z and determine whether the circuit is Mealy or Moore:



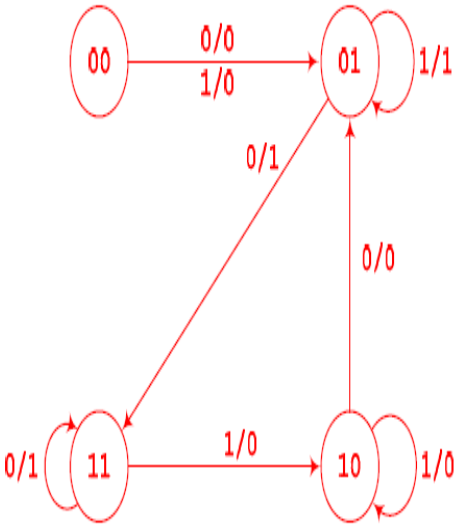
The circuit is Mealy since the output depends on both the current state and the input.

$$D_A = \overline{\overline{(XQ_A)}\,\overline{(\bar{X}Q_B)}} = XQ_A + \bar{X}Q_B$$

$$D_B = \overline{Q_A} + \bar{X}$$

$$Z = Q_B(\overline{Q_A} + \bar{X}) = \overline{Q_A}Q_B + \bar{X}Q_B$$

Q_A	Q_B	X	Q_A^+	Q_B^+	Z
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	1	1	1
0	1	1	0	1	1
1	0	0	0	1	0
1	0	1	1	0	0
1	1	0	1	1	1
1	1	1	1	0	0



(ii) Complete the following waveform for the positive-edge triggered circuit that implements the state diagram provided below. Assume the circuit is initially at the state $Q_1Q_0 = 00$.