**Name: KEY** **Id#**

# COE 202, Term 121
# Digital Logic Design

## Quiz# 5

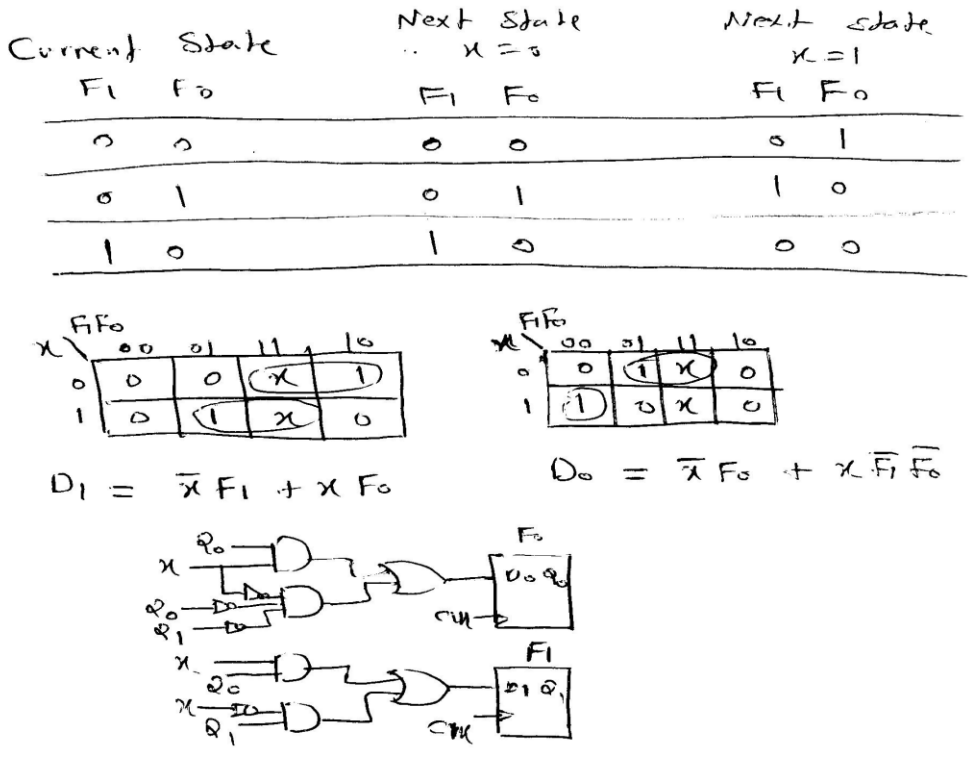
Date: Saturday, Dec. 22

**Q1.** The state table of a sequential circuit which has a single input X and two outputs, which are the flip flop outputs, is given below.

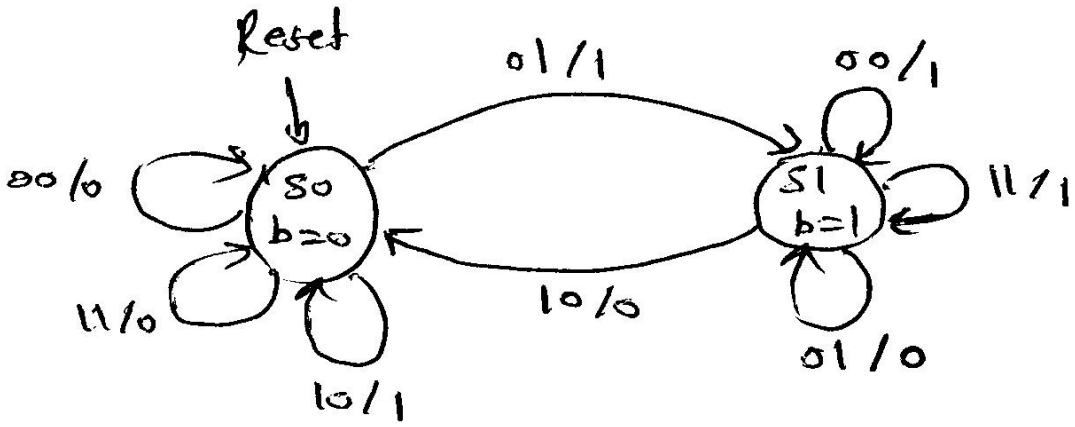
| Current State | Next State X=0 | Next State X=1 |
|---|---|---|
| S0 | S0 | S1 |
| S1 | S1 | S2 |
| S2 | S2 | S0 |

(i) Implement the sequential circuit using D-FFs and the smallest number of gates possible assuming the state assignment: S0=00, S1=01, and S2=10. Minimize your equations using K-map method.

(ii) Draw the circuit diagram.



**Q2**. It is required to design a sequential circuit that receives two unsigned numbers X and Y serially and computes the output Z=X-Y serially, assuming that $X \geq Y$. Derive the state diagram for your circuit assuming **Mealy** model.



**Q3**. It is required to design a sequential circuit that receives a serial input X and produces a serial output Z. The output Z will be 1 when the circuit detects the sequence 1010 assuming overlapping sequence detection. Derive the state diagram for your circuit assuming **Moore** model.