Name: KEY **Id#**

COE 202, Term 112
Digital Logic Design

Quiz# 5

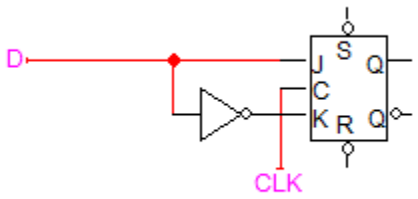
Date: Wednesday, April 25

Q1. Design a rising edge-triggered D flip-flop using a rising edge-triggered JK flip flop.

State Table:

Current State (Q)	Input (D)	Next State (Q)	J	K
0	0	0	0	X
0	1	1	1	X
1	0	0	X	1
1	1	1	X	0

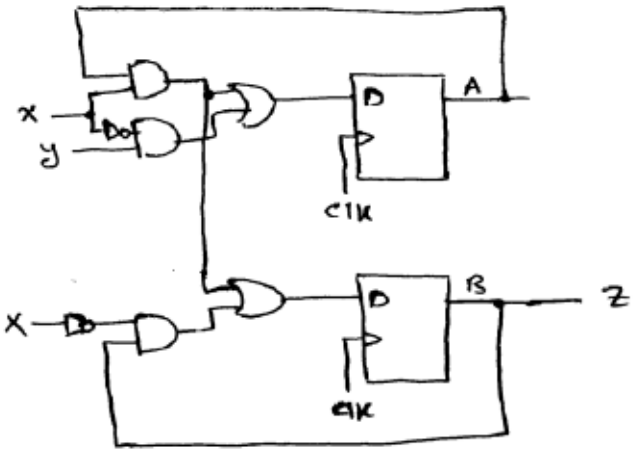
J= D K=D'



Q2. A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following equations:

$D_A = X` Y + X A$ $D_B = X` B + X A$ $Z = B$

(i) Draw the logic diagram of the circuit.



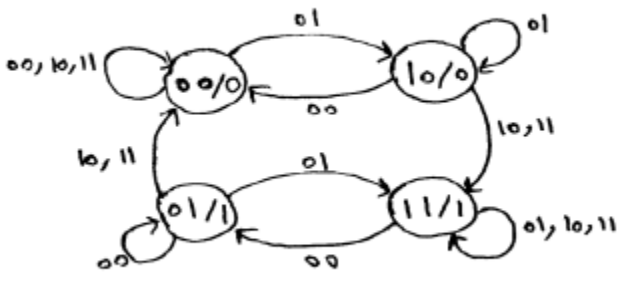
(ii) Derive the state table.

State Table:

Current State AB	Next State xy=00 AB	xy=01 AB	xy=10 AB	xy=11 AB	output z
0 0	0 0	1 0	0 0	0 0	0
0 1	0 1	1 1	0 0	0 0	1
1 0	0 0	1 0	1 1	1 1	0
1 1	0 1	1 1	1 1	1 1	1

(iii) Derive the state diagram.

State Diagram:



* Note that this circuit has a Moore model.
* Note that this circuit has several synchronizing sequence For example, {00, 11} synchronizes it to state 00.