Name: KEY Id#

COE 202, Term 112

Digital Logic Design

Quiz# 5

 Date: Wednesday, April 25

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# **Q1**. Design a rising edge-triggered D flip-flop using a rising edge-triggered JK flip flop.

 State Table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Current State (Q) | Input (D) | Next State (Q) | J | K |
| 0 | 0 | 0 | 0 | X |
| 0 | 1 | 1 | 1 | X |
| 1 | 0 | 0 | X | 1 |
| 1 | 1 | 1 | X | 0 |

J= D K=D’



# **Q2**. A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following equations:

DA = X` Y + X A DB = X` B + X A Z = B

1. Draw the logic diagram of the circuit.



## Derive the state table.



## Derive the state diagram.

