Name: KEY **Id#**

COE 202, Term 102
Fundamentals of Computer Engineering

Quiz# 5 (Take Home)

Due date: Saturday, May 7, 2011

Q.1. It is required to design a 4-bit arithmetic and logic unit that has two 4-bit inputs $\mathbf{A=A_3A_2A_1A_0}$ and $\mathbf{B=B_3B_2B_1B_0}$ and one **6-bit output** $\mathbf{C= C_5C_4C_3C_2C_1C_0}$. The circuit implements the following functions based on the values of the four selection inputs S3, S2, S1 and S0.

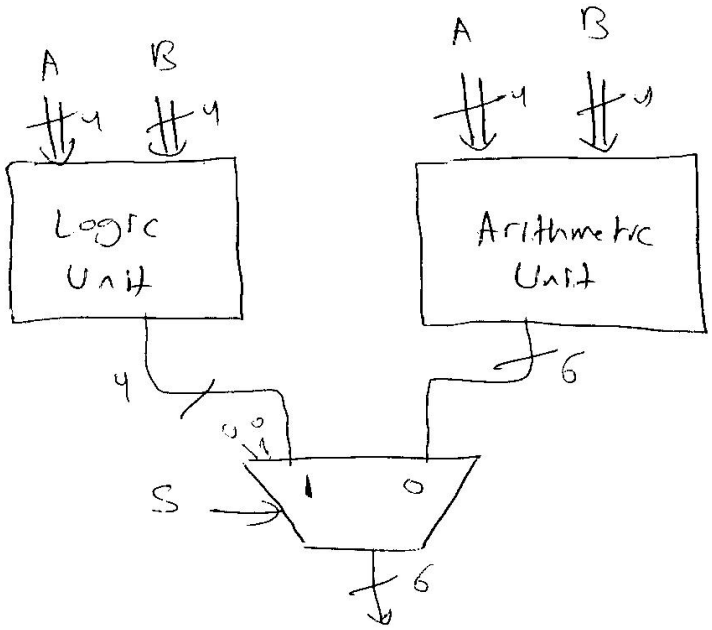
S3 S2 S1 S0	Function
0 0 0 0	C = A + B
0 0 0 1	C = A – B
0 0 1 0	C = A+1
0 0 1 1	C = A-1
0 1 0 0	C = A+ 2
0 1 0 1	C = A – 2
0 1 1 0	C = B
0 1 1 1	C = -B
1 0 0 0	C = 2B
1 0 0 1	C = 3B
1 0 1 0	C = 4B
1 0 1 1	C = A and B
1 1 0 0	C = A or B
1 1 0 1	C = A xor B
1 1 1 0	C = A xnor B
1 1 1 1	C = not B

(i) Show the block diagram design of your circuit using MSI components like Adder, Multiplexor, as needed.

(ii) Model your design in logic works.

(iii) Test your design and verify its correctness by simulation. Show snapshots of your simulation to demonstrate its correctness. For each function, test at least 4 input combinations of your choice to demonstrate correct functionality.

We partition the design of the Arithmetic & logic unit into arithmetic unit and logic unit and we select between their outputs as shown below:

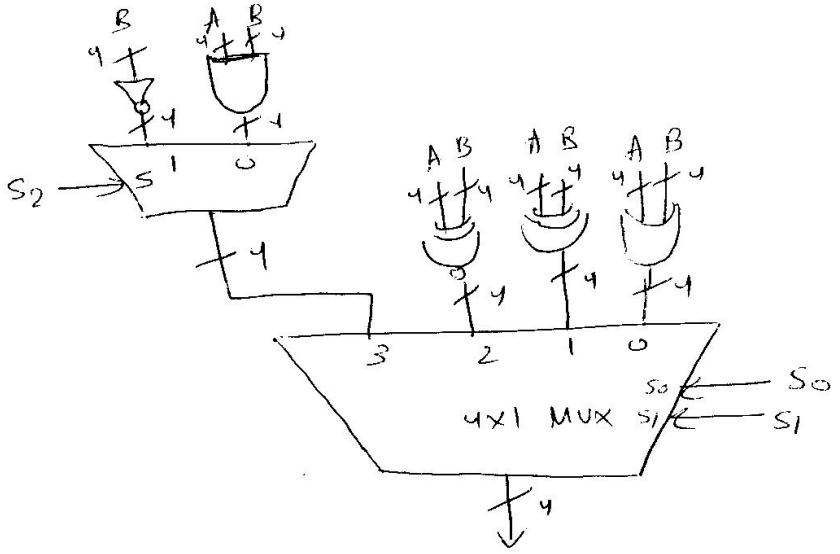


We design the select function as follows:

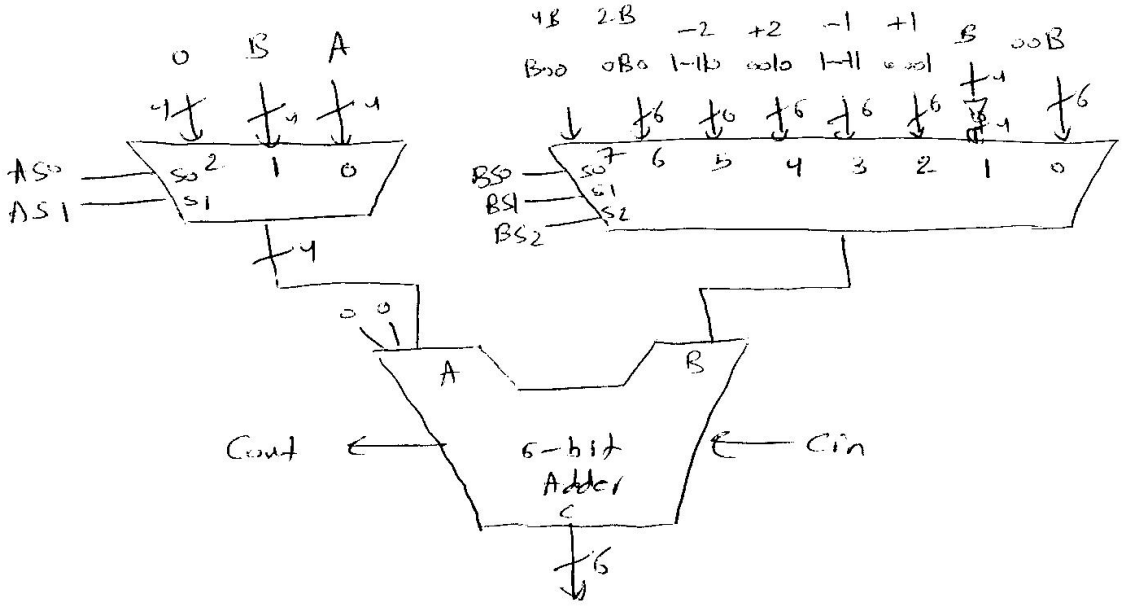
S_3S_2 \ S_1S_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	0

$$S = S_3 S_2 + S_3 S_1 S_0$$

Next, we design the logic unit as follows:



The Arithmetic unit is designed as follows using one 6-bit adder:



After that, we need to find out the equations for C_{in}, A_{S1}, A_{S0}, B_{S2}, B_{S1}, and B_{S0}.

C_{in}

S_3S_2 \ S_1S_0	00	01	11	10
00	0	1	0	0
01	0	0	1	0
11	0	0	0	0
10	0	0	0	0

$$C_{in} = \overline{S_3}\, S_2 S_1 S_0 + \overline{S_3}\overline{S_2}\overline{S_1} S_0$$
$$= \overline{S_3} S_0 (S_2 S_1 + \overline{S_2}\,\overline{S_1})$$
$$= \overline{S_3} S_0 \overline{(S_1 \oplus S_2)}$$

A_{S1}

S_3S_2 \ S_1S_0	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	0	0	0
10	1	0	0	1

$$A_{S1} = \overline{S_3} S_2 S_1 + S_3 \overline{S_2}\,\overline{S_0}$$

A_{S0}

S_3S_2 \ S_1S_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0	0	0
10	0	1	0	0

$$A_{S0} = S_3 \overline{S_2}\,\overline{S_1} S_0$$

BS2

S_3S_2 \ S_1S_0	00	01	11	10
00	0	0	0	0
01	1	1	0	0
11	0	0	0	0
10	1	1	0	1

$$BS2 = \overline{S_3}\,S_2\overline{S_1} + S_3\overline{S_2}\,\overline{S_1} + S_3\overline{S_2}\,\overline{S_0}$$

BS1

S_3S_2 \ S_1S_0	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	0	0	0	0
10	1	1	0	1

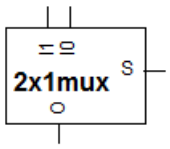
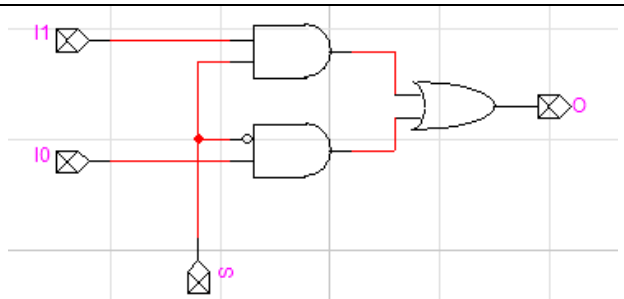
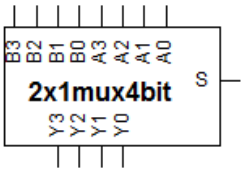
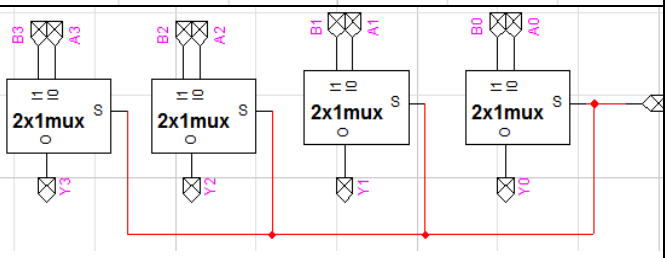
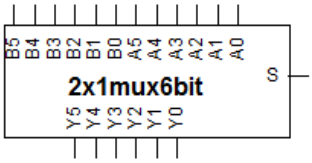
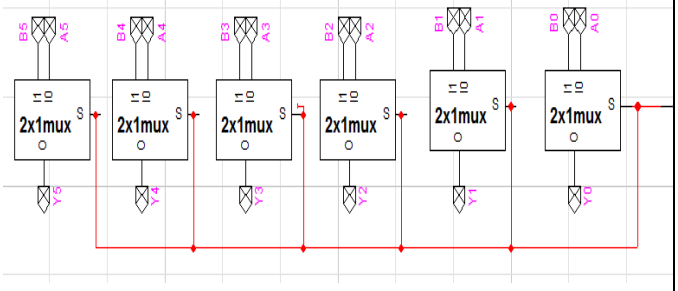
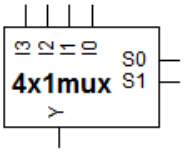
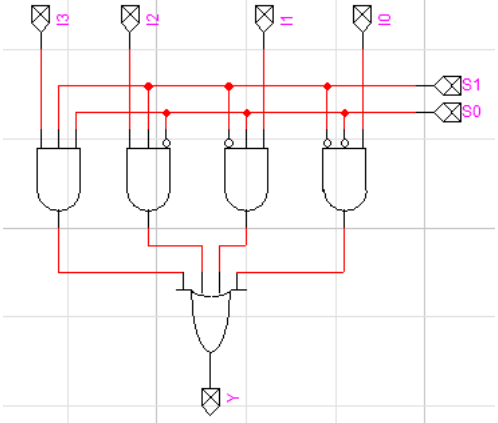
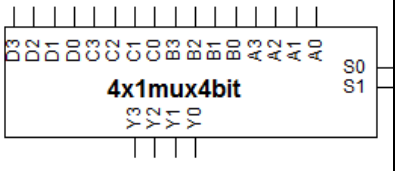
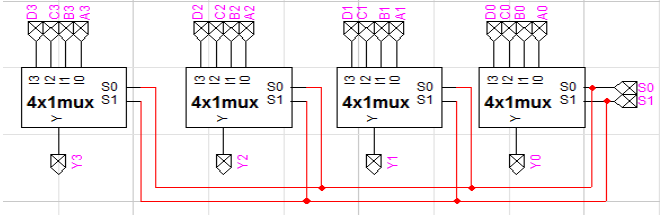
$$BS1 = \overline{S_3}\,\overline{S_2}S_1 + S_3\overline{S_2}\,\overline{S_0} + S_3\overline{S_2}\,\overline{S_1}$$

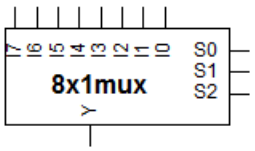
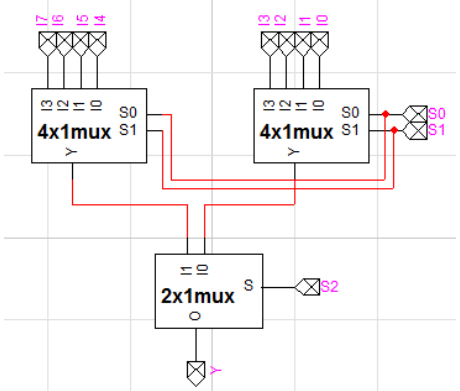
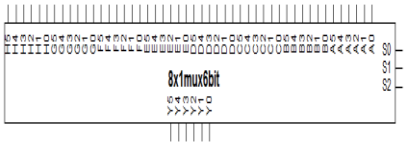
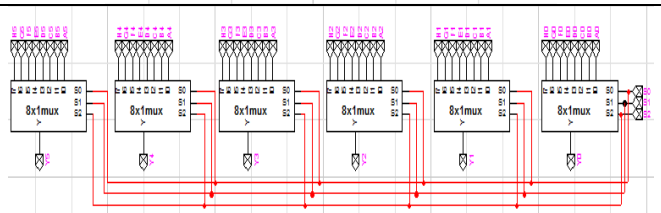
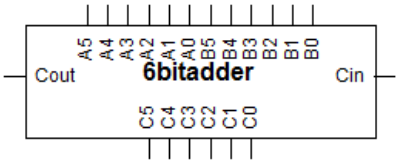
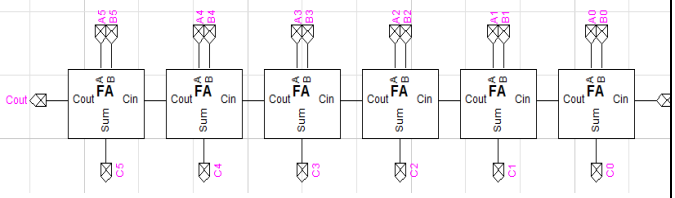
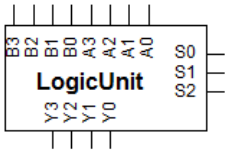
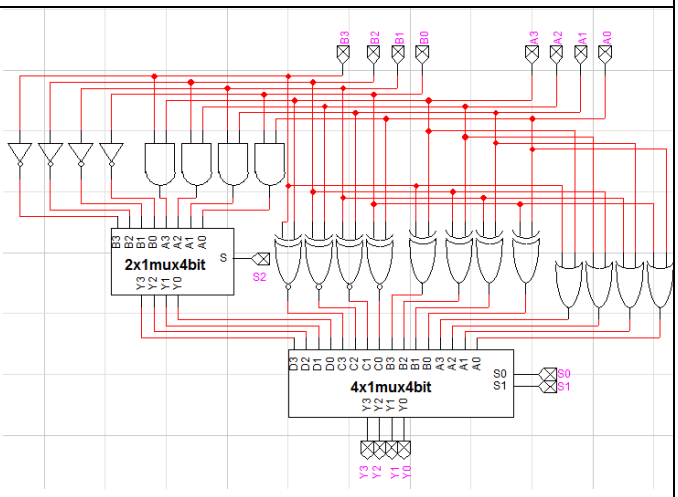
BS0

S_3S_2 \ S_1S_0	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	0	0	0	0
10	0	0	0	1

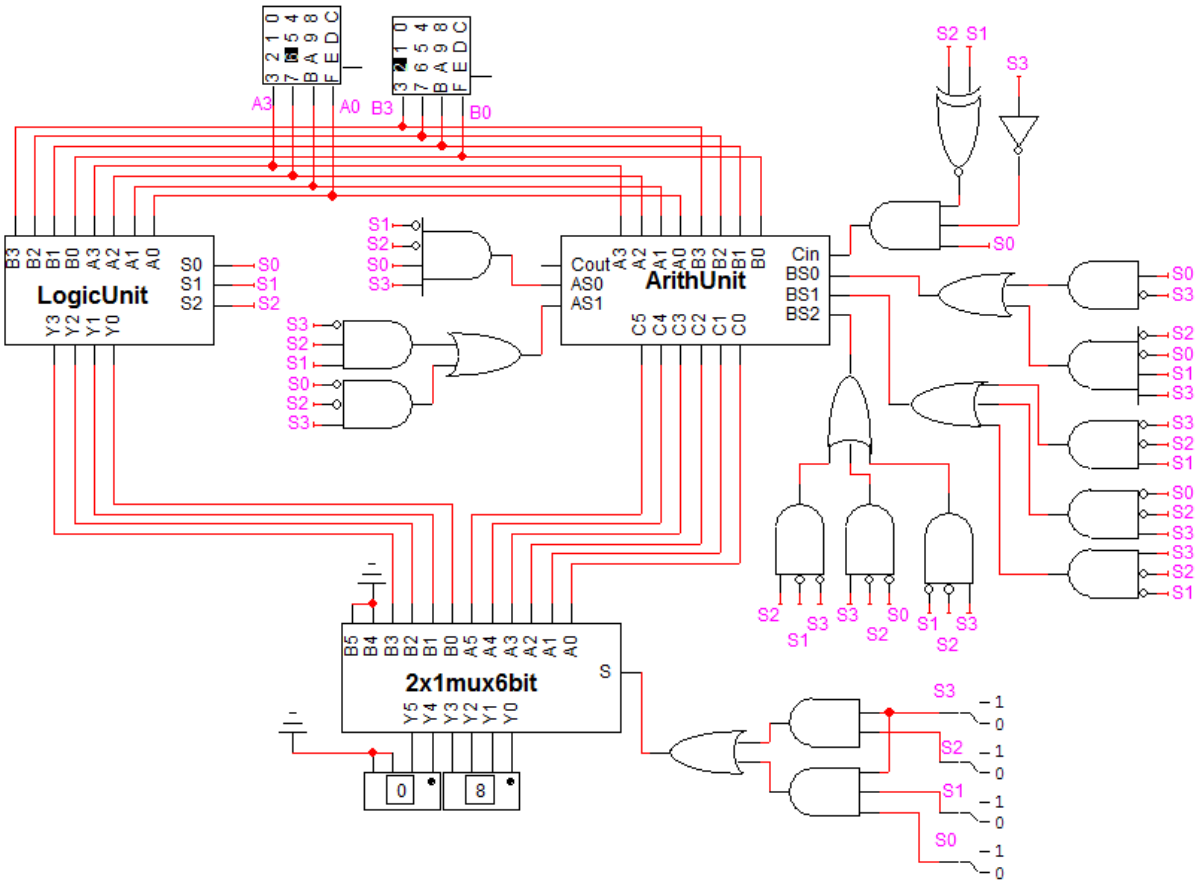
$$BS0 = \overline{S_3}\,S_0 + S_3\overline{S_2}\,S_1\overline{S_0}$$

The design has been implemented in logic works and the following devices were created:

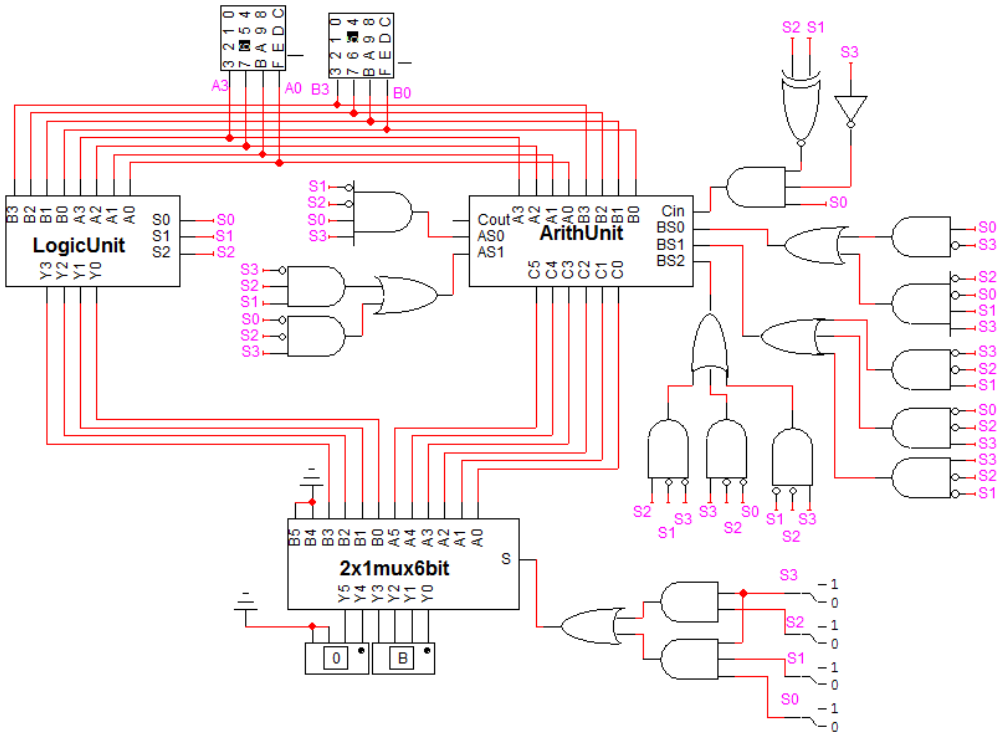
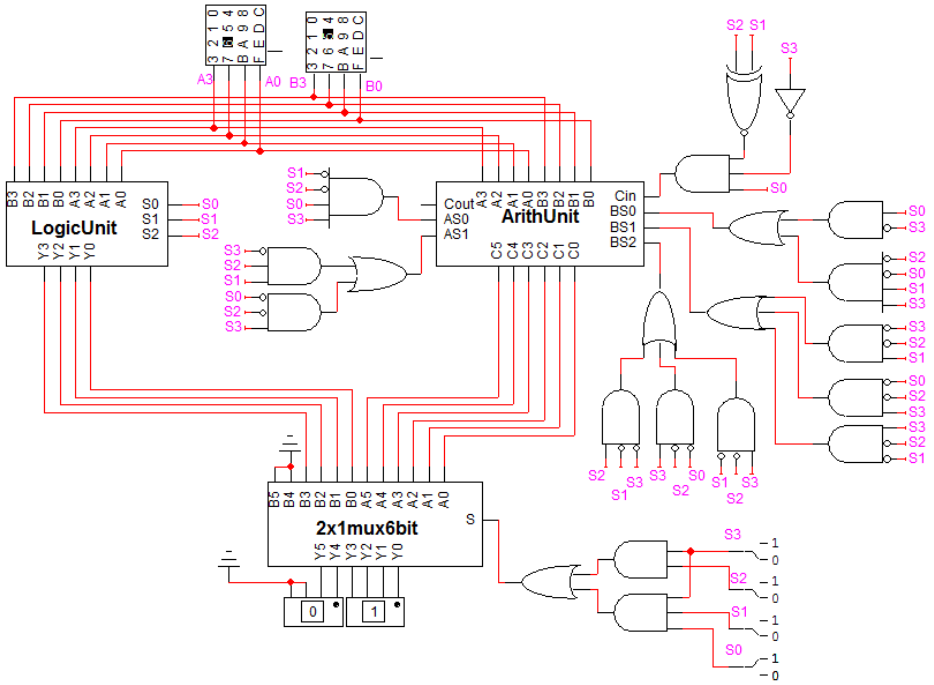
Device Name	Device Symbol	Logic Diagram
2x1 mux		
2x1mux4bit		
2x1mux6bit		
4x1mux		
4x1mux4bit		

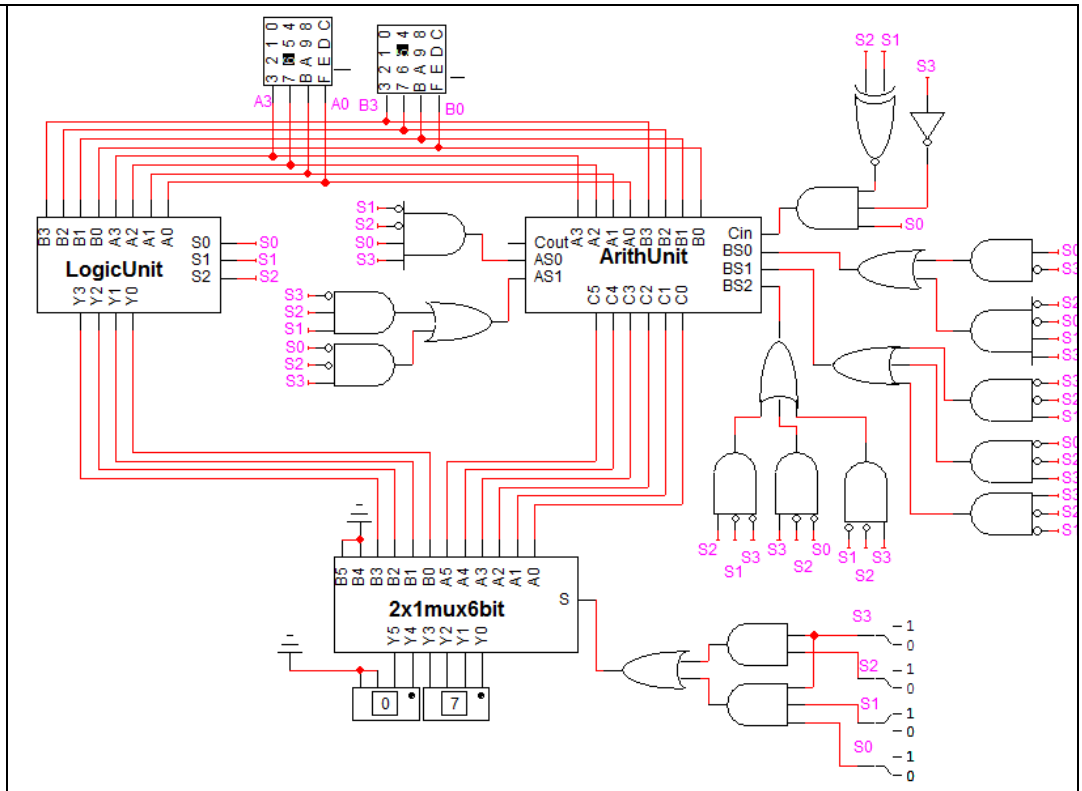
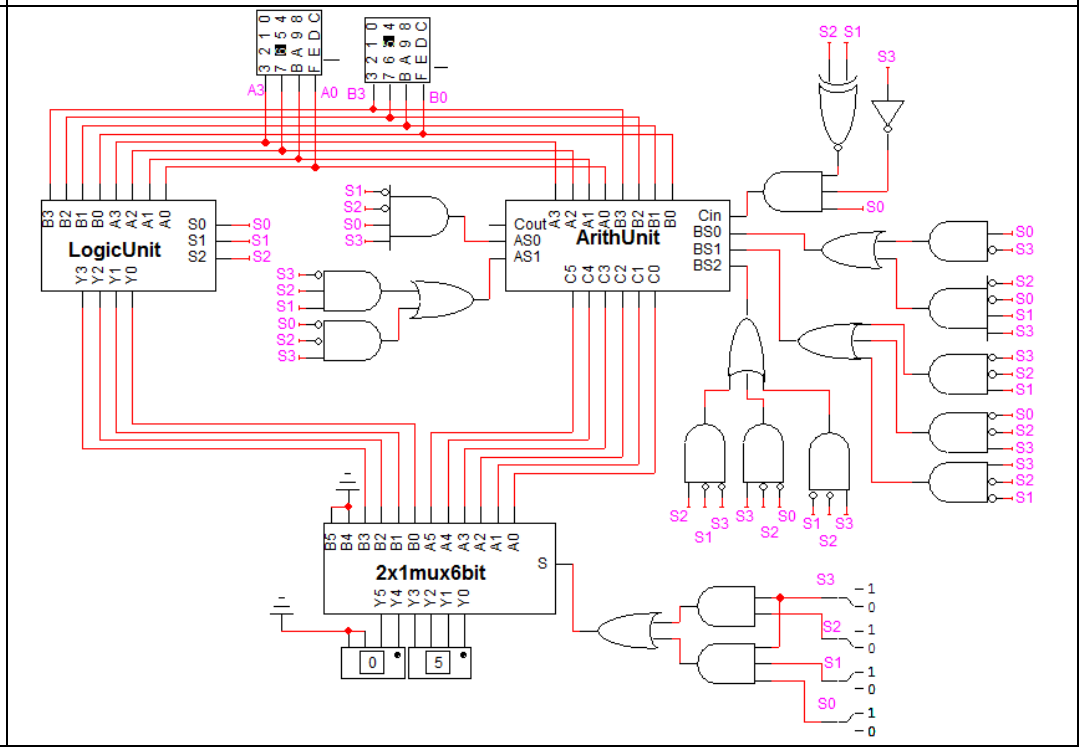
8x1mux		
8x1mux6bit		
6bitadder		
LogicUnit		

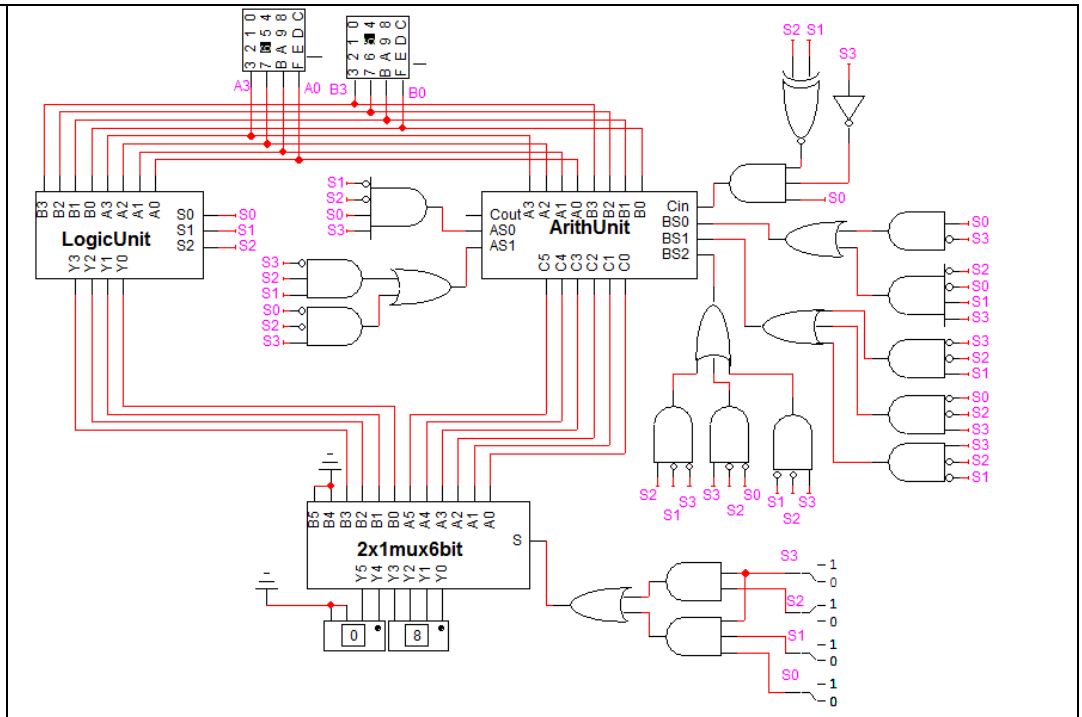
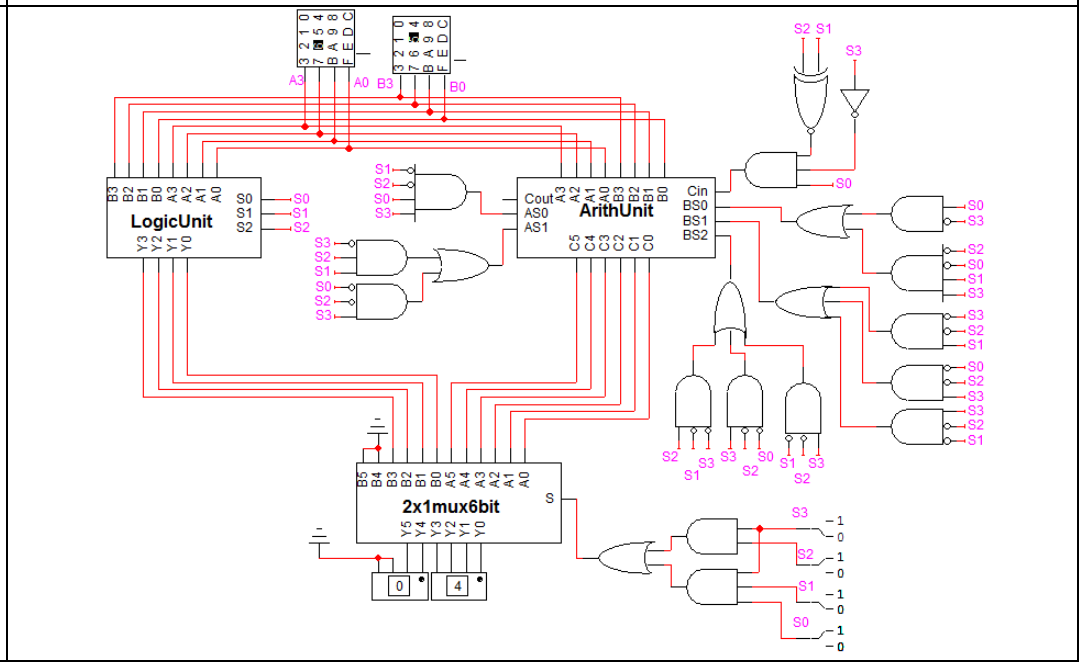
The whole ALU after integrating all the components and adding input and output is shown below:

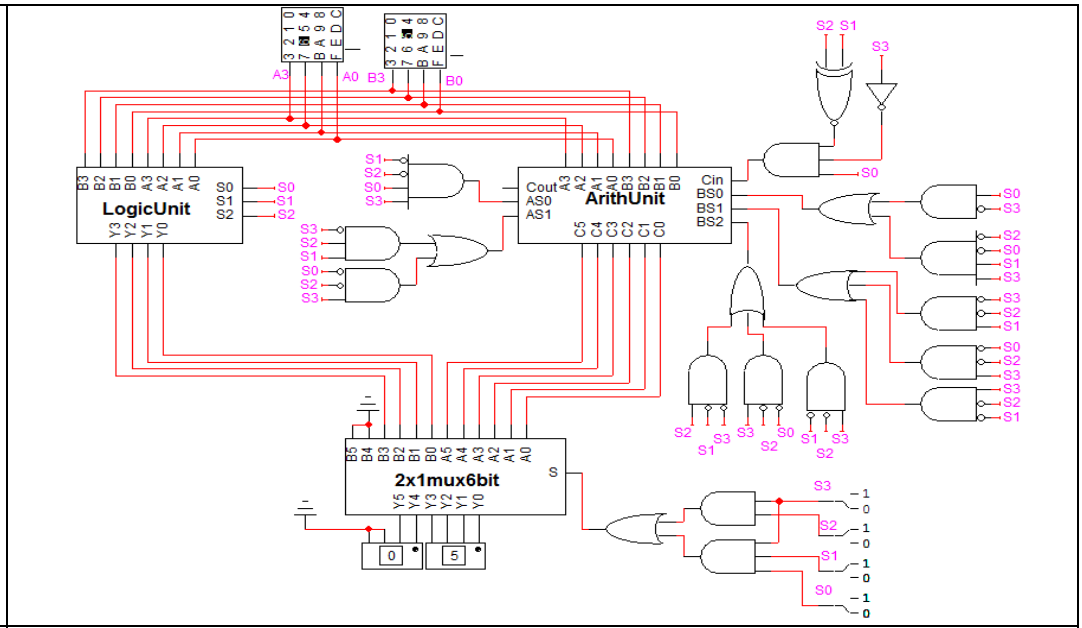
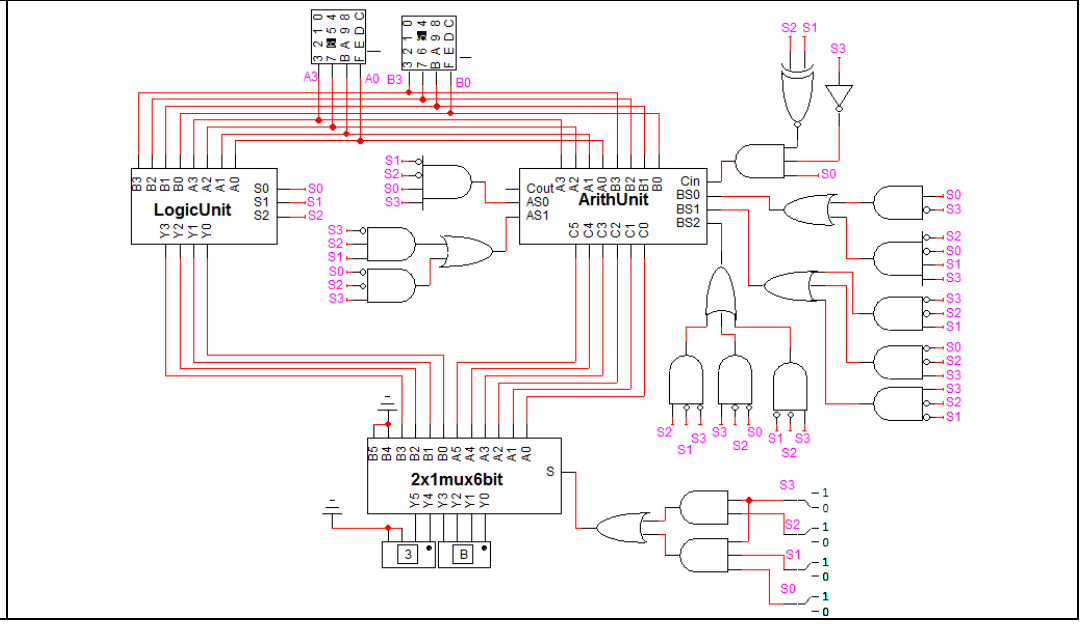


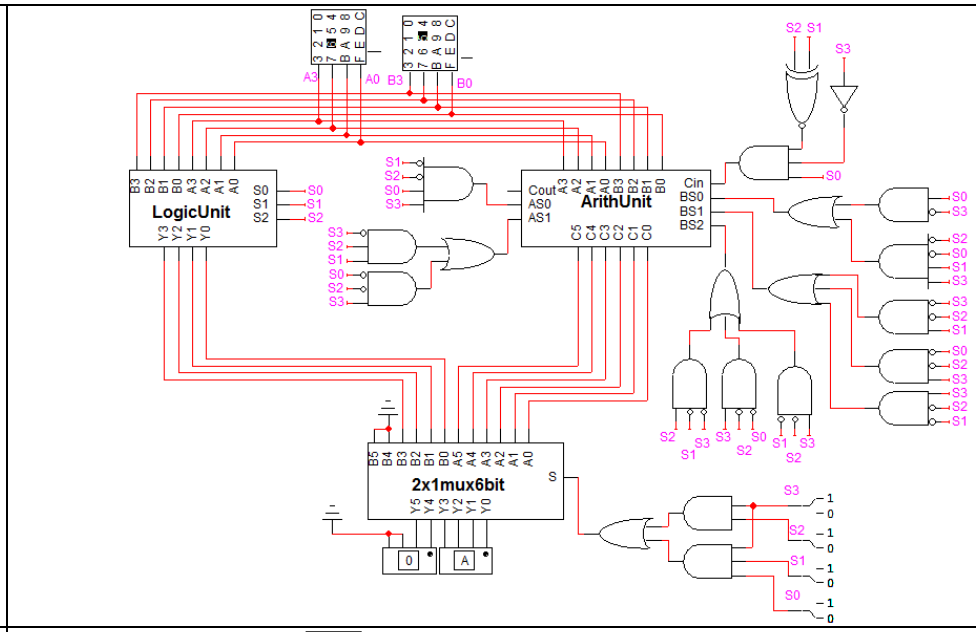
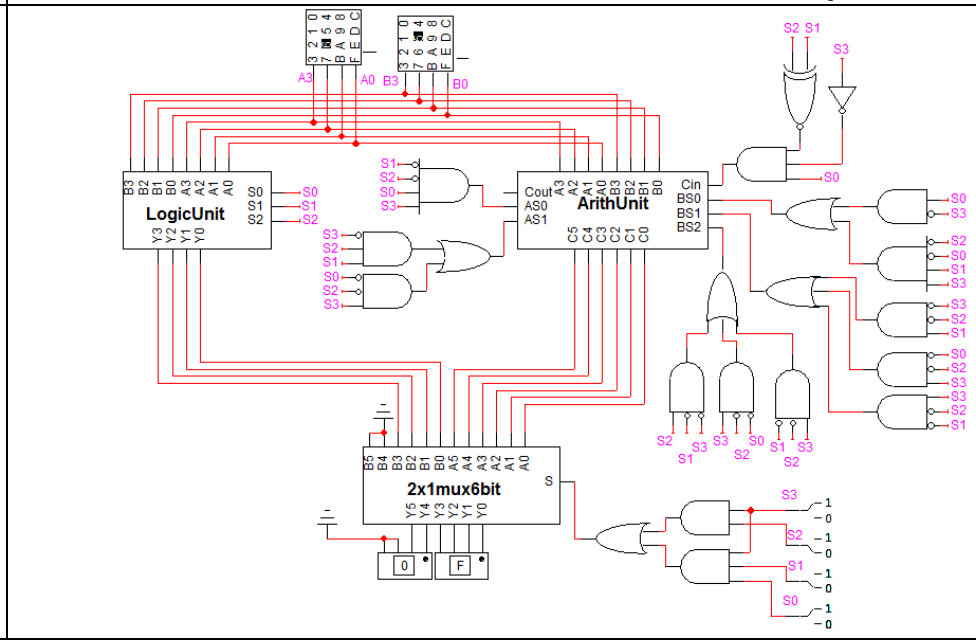
We will show next Verification of correct functionality of the ALU by setting A=6 and B=5:

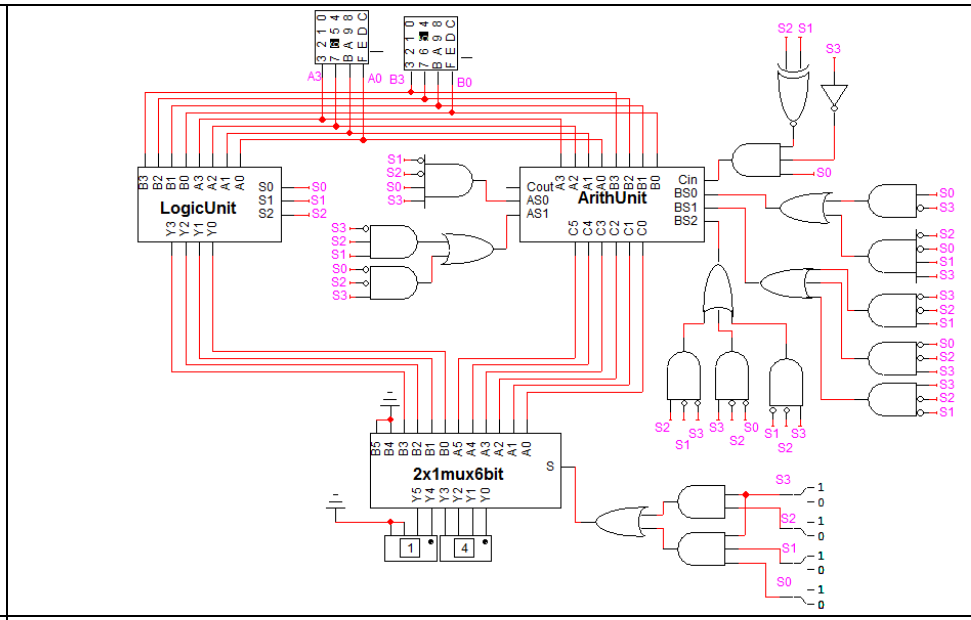
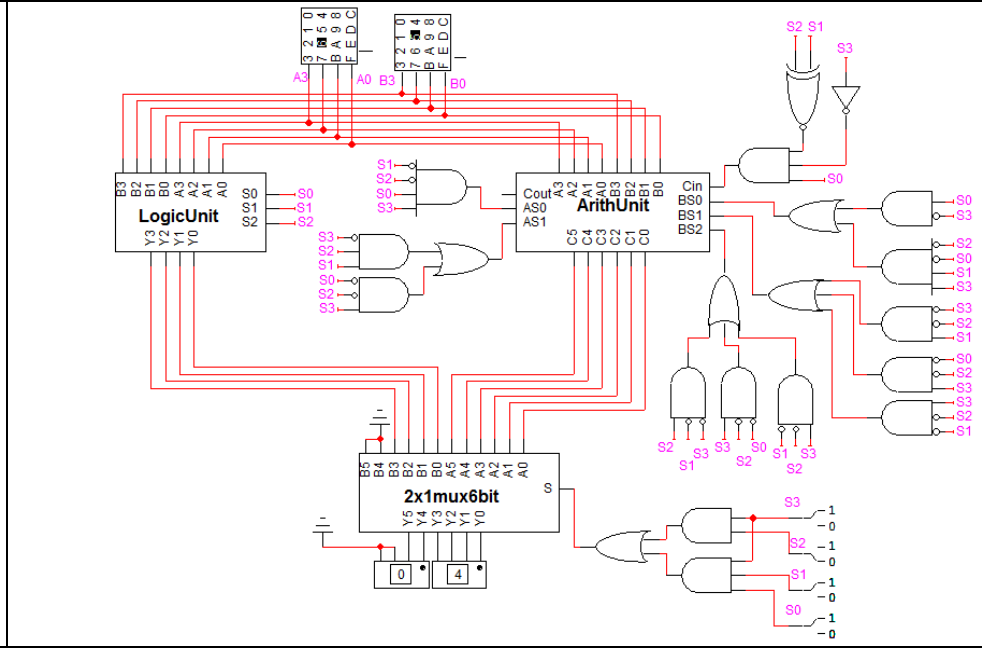
Function	Verification
C = A + B	
C = A – B	

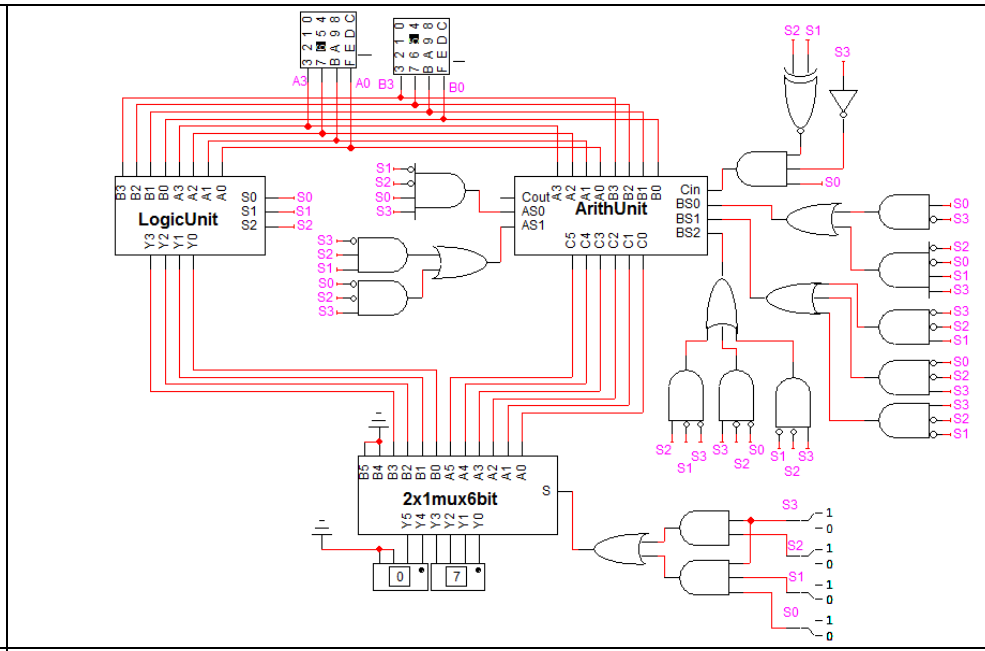
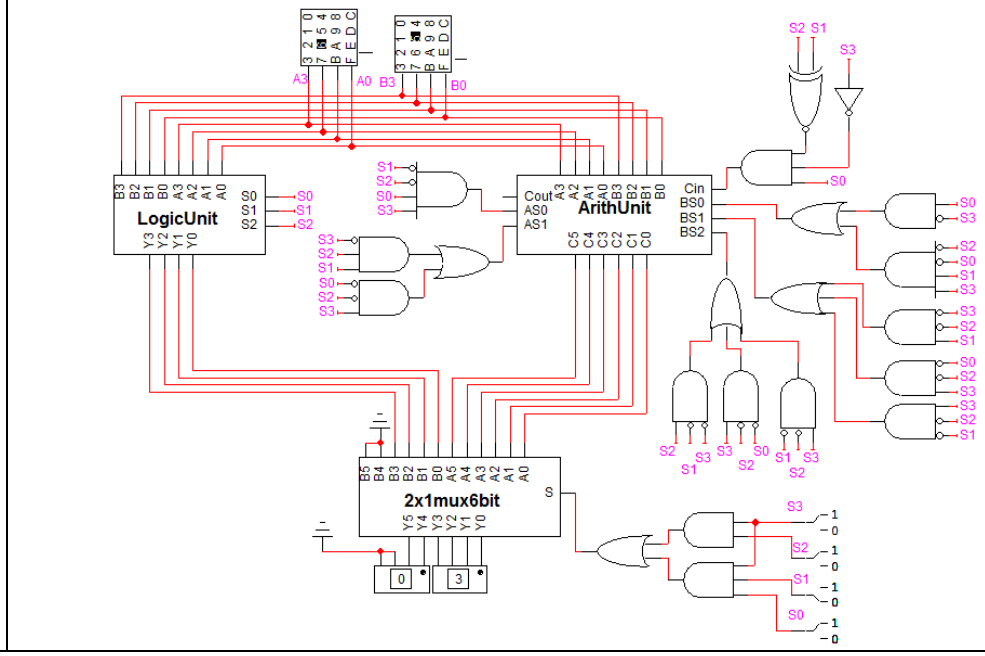
C = A+1	 LogicUnit ArithUnit 2x1mux6bit Cout AS0 AS1 Cin BS0 BS1 BS2 S0 S1 S2 S3 A3 A0 B3 B0 0 7
C = A-1	 LogicUnit ArithUnit 2x1mux6bit Cout AS0 AS1 Cin BS0 BS1 BS2 S0 S1 S2 S3 A3 A0 B3 B0 0 5

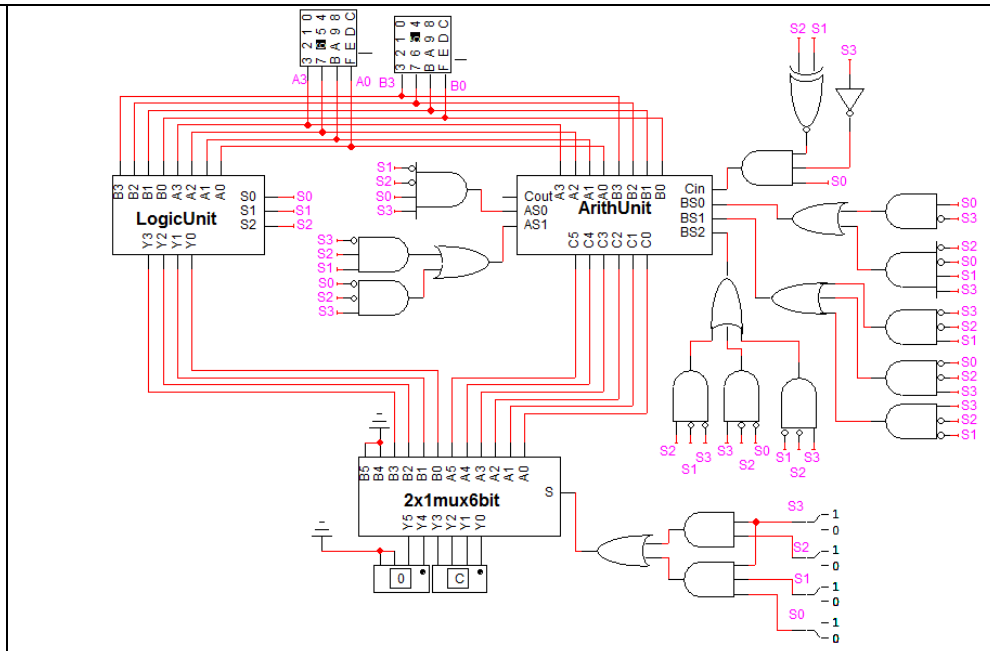
C = A+ 2	 LogicUnit ArithUnit 2x1mux6bit A3 A0 B3 B0 S2 S1 S3 S0 0 8
C = A – 2	 LogicUnit ArithUnit 2x1mux6bit A3 A0 B3 B0 S2 S1 S3 S0 0 4

C = B	 LogicUnit ArithUnit 2x1mux6bit Cout AS0 AS1 Cin BS0 BS1 BS2 S0 S1 S2 S3 0 5
C = -B	 LogicUnit ArithUnit 2x1mux6bit Cout AS0 AS1 Cin BS0 BS1 BS2 S0 S1 S2 S3 3 B

C = 2B	 LogicUnit ArithUnit 2x1mux6bit Cout AS0 AS1 Cin BS0 BS1 BS2 S 0 A
C = 3B	 LogicUnit ArithUnit 2x1mux6bit Cout AS0 AS1 Cin BS0 BS1 BS2 S 0 F

C = 4B	 LogicUnit ArithUnit 2x1mux6bit
C = A and B	 LogicUnit ArithUnit 2x1mux6bit

C = A or B	
C = A xor B	

C = A xnor B	
C = not B