Name: KEY **Id#**

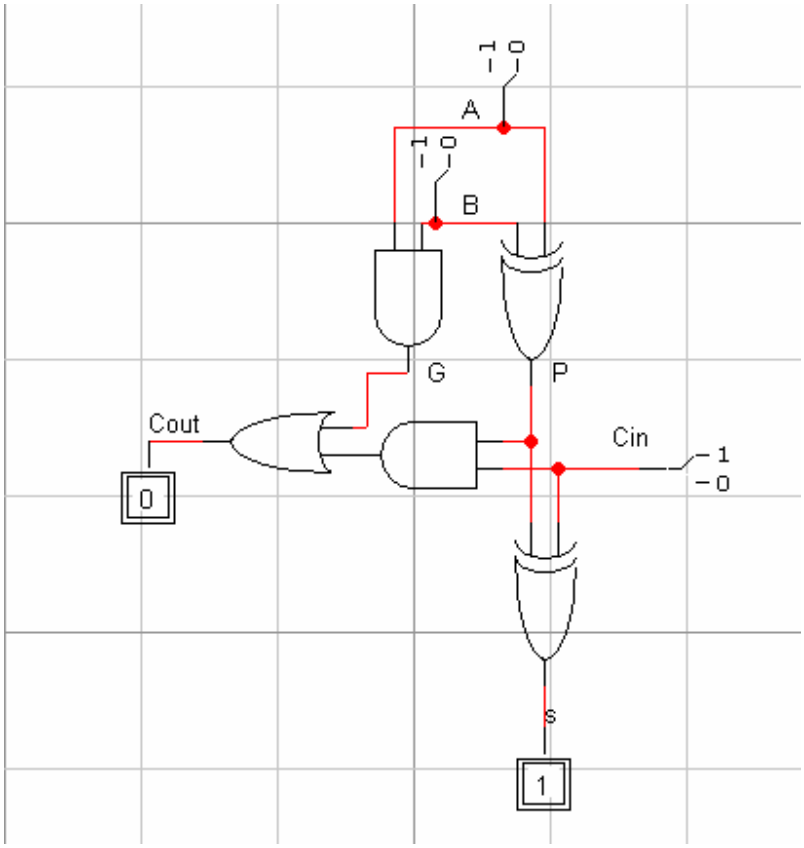
COE 202, Term 052
Fundamentals of Computer Engineering

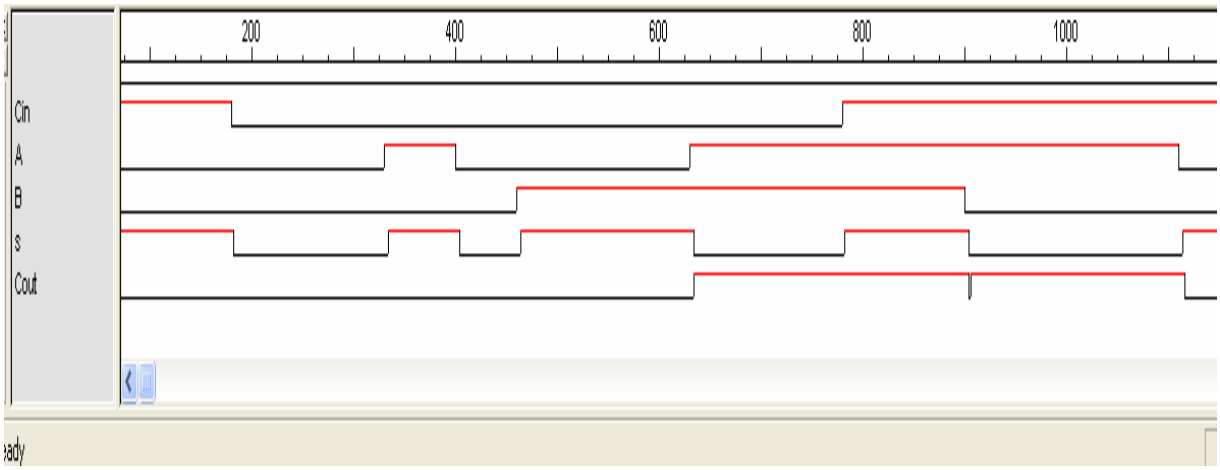
Quiz# 5 (Take Home)

Due date: Monday, April 17, 2006

Q.1. Assume the delay of a gate is equal to the number of its inputs, i.e. the delay of a 2-input gate is 2, and the delay of a 3-input gate is 3. Using Logic works do the following:

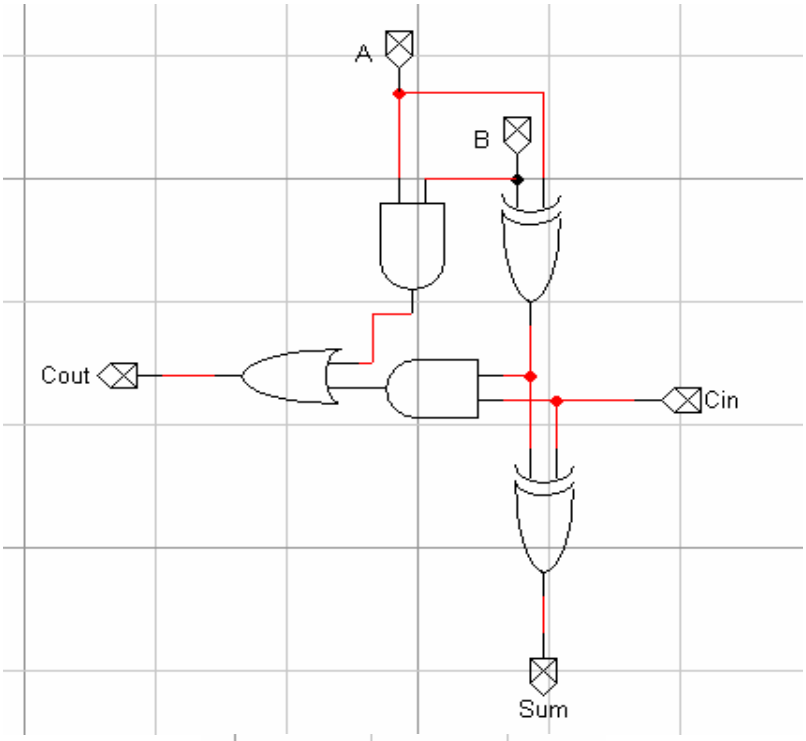
a. Model a full-adder.

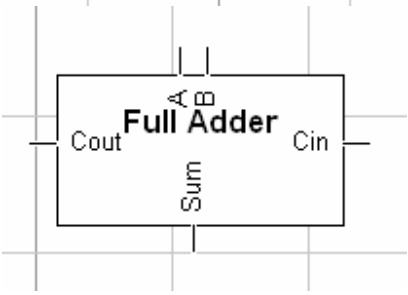


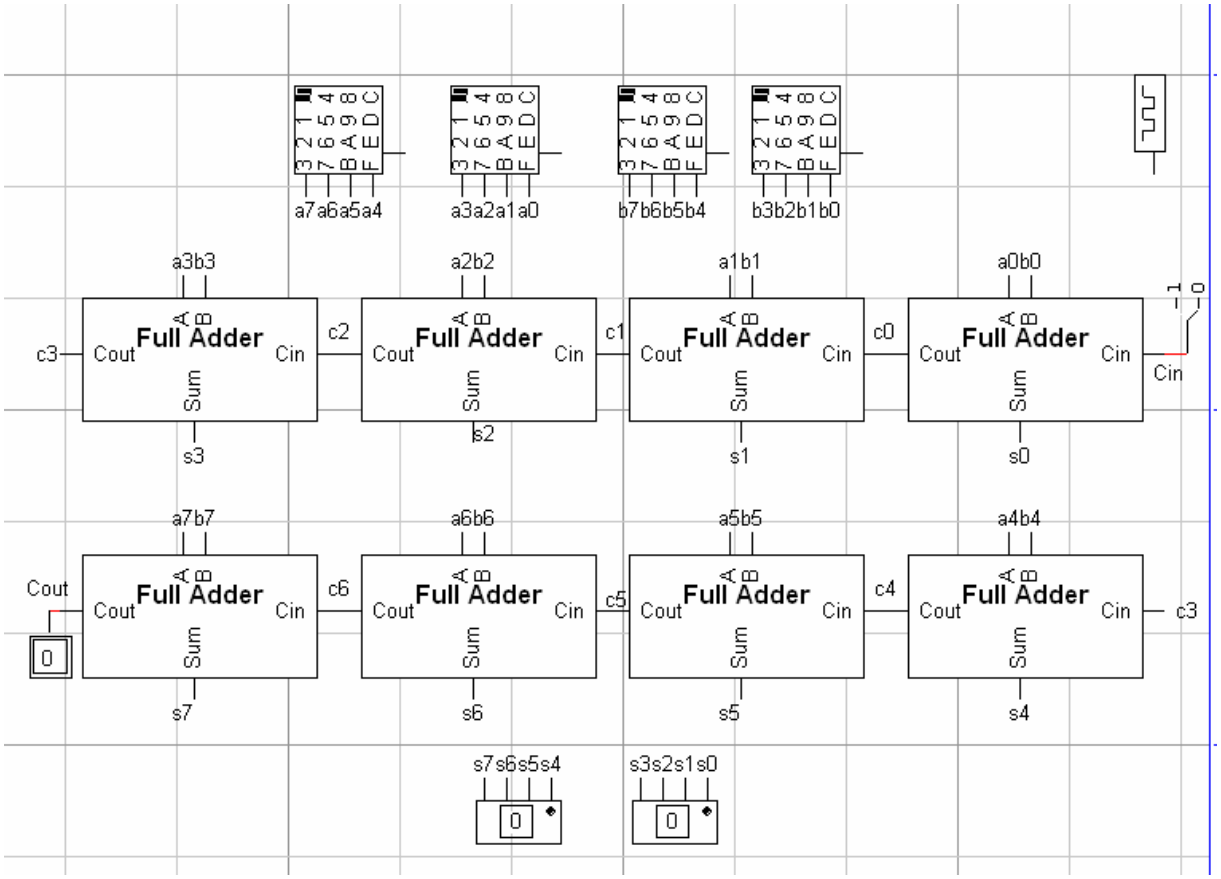


b. Use the full adder model and construction from it an 8-bit Ripple Carry Adder.

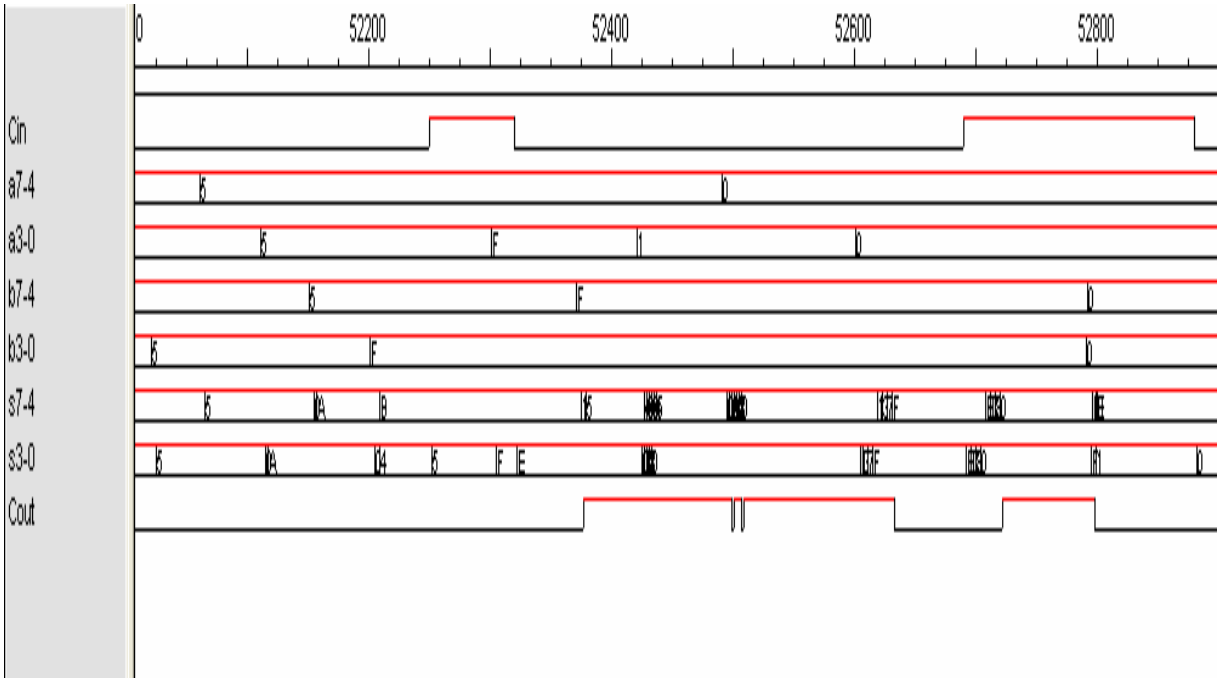
In order to simplify the modeling process, we will create a symbol for the full adder cell and then connect 8 copies of it as shown below. We first connect input and output ports then create the symbol.


A
B
Cout
Cin
Sum


A
B
Full Adder
Cout
Cin
Sum

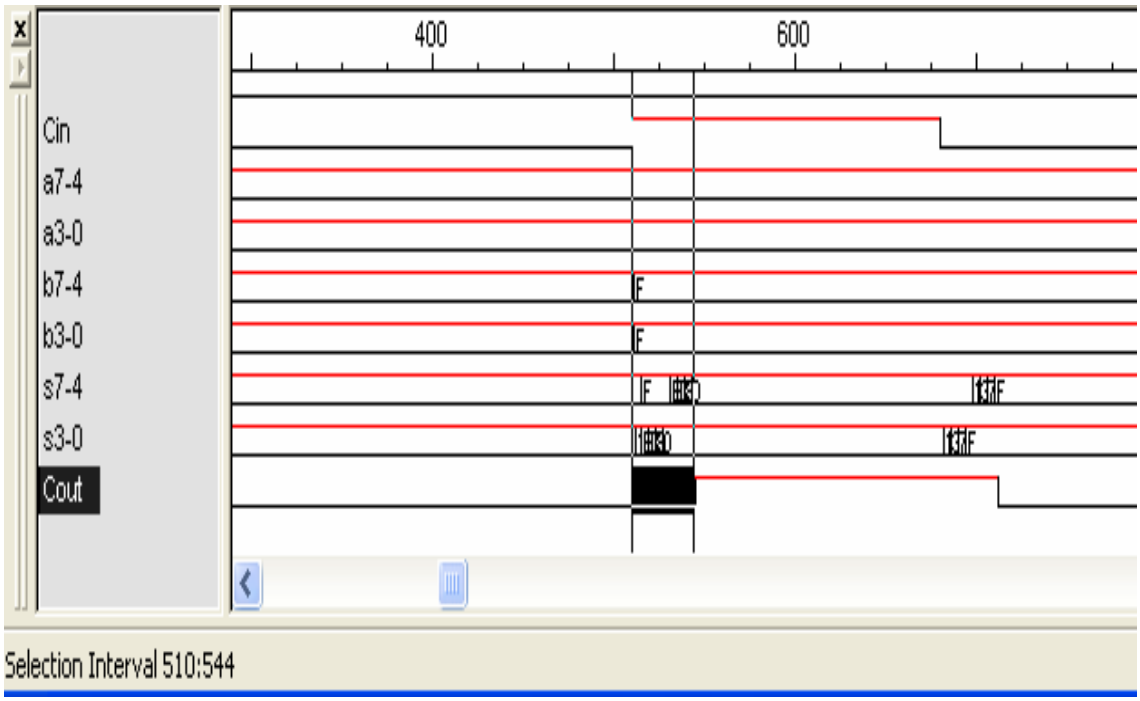


The simulation waveform that illustrates that the adder works properly is shown below:



c. Determine the worst case delay in your 8-bit Ripple Carry Adder by simulation.

The worst case delay is when the A & B inputs have propoagation condition and the Cin signal is changing from 0 to 1 or from 1 to 0. The Cout signal will change accordingly after a delay equal 2+4*8=34 ns. This is exactly what is obtained by simulation as shown below.



As can be seen, the delay from the Cin signal to the Cout signal is 544-510= 34ns.

d. Model a 4-bit Carry Look Ahead adder.

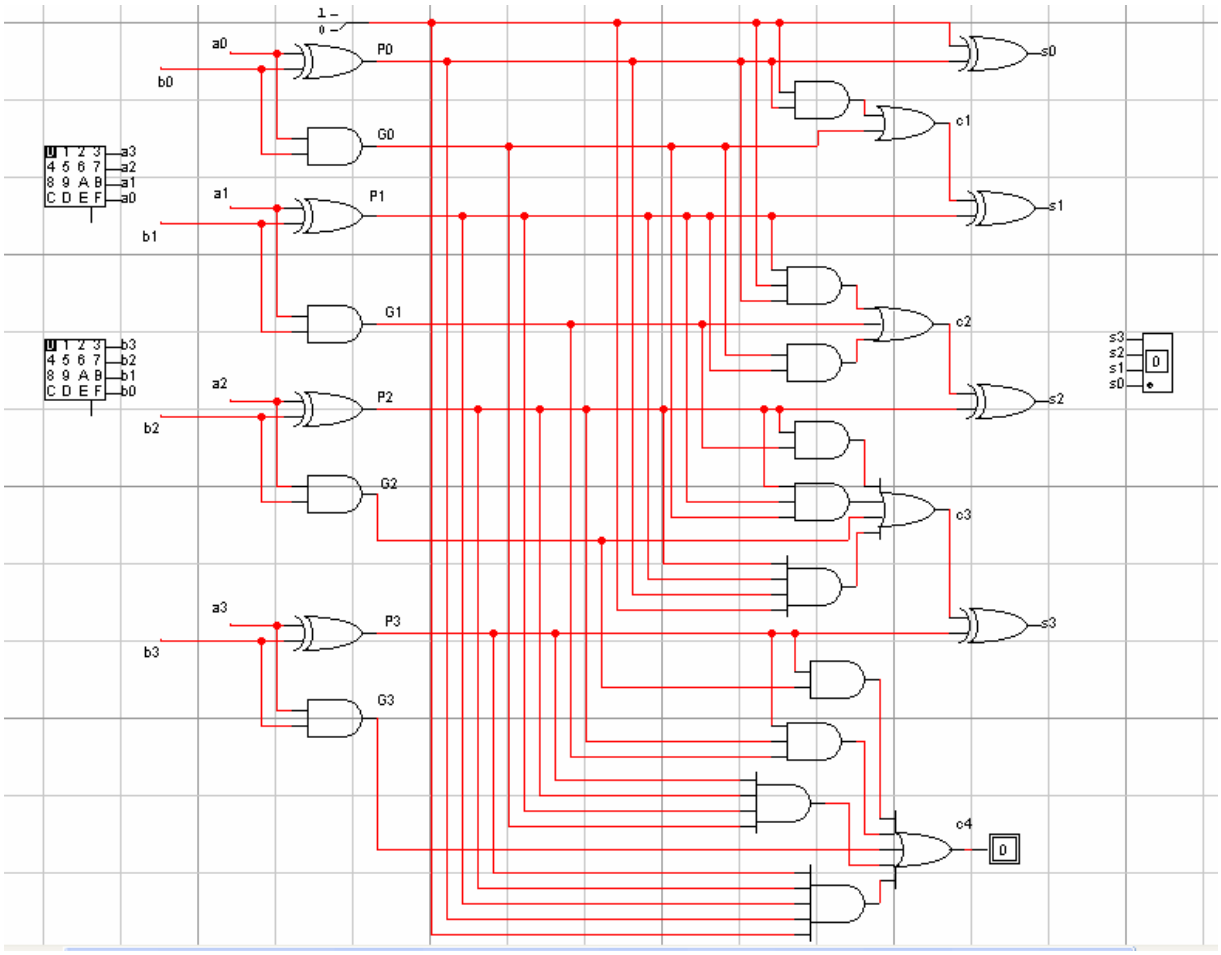
The 4-bit carry look ahead adder is modeled as shown below.

P0 = A0 ⊕ B0 ; G0= A0 AND B0
S0 = P0 ⊕ C0
C0 = G0 + C0 P0

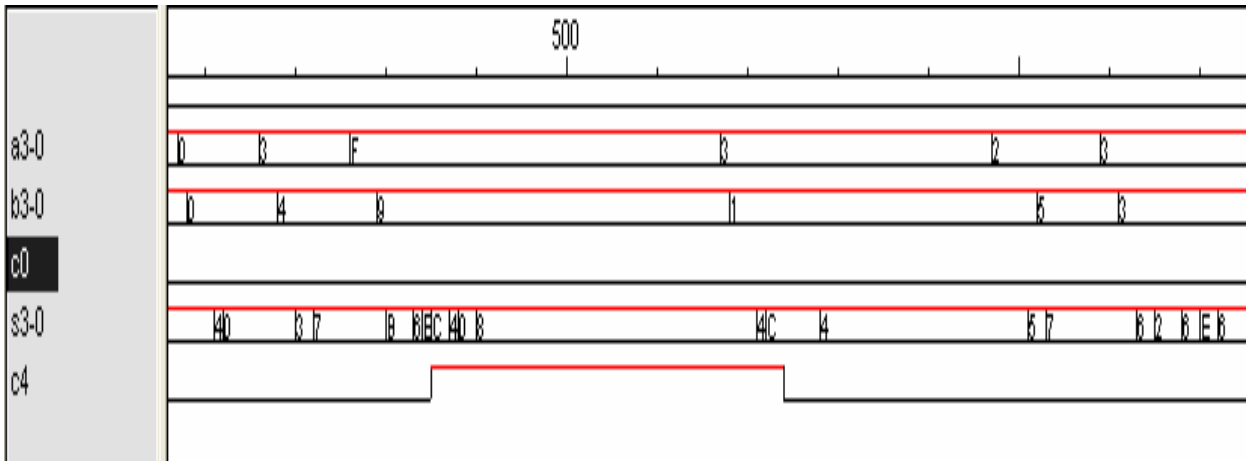
P1 = A1 ⊕ B1 ; G1= A1 AND B1
S1 = P1 ⊕ C1
C1 = G1 + G0 P1 + C0 P0 P1

P2 = A2 ⊕ B2 ; G2= A2 AND B2
S2 = P2 ⊕ C2
C1 = G2 + G1 P2 + G0 P1 P2 + C0 P0 P1 P2

P3 = A3 ⊕ B3 ; G3= A3 AND B3
S3 = P3 ⊕ C3
C3 = G3 + G2 P3 + G1 P2 P3 + G0 P1 P2 P3 + C0 P0 P1 P2 P3

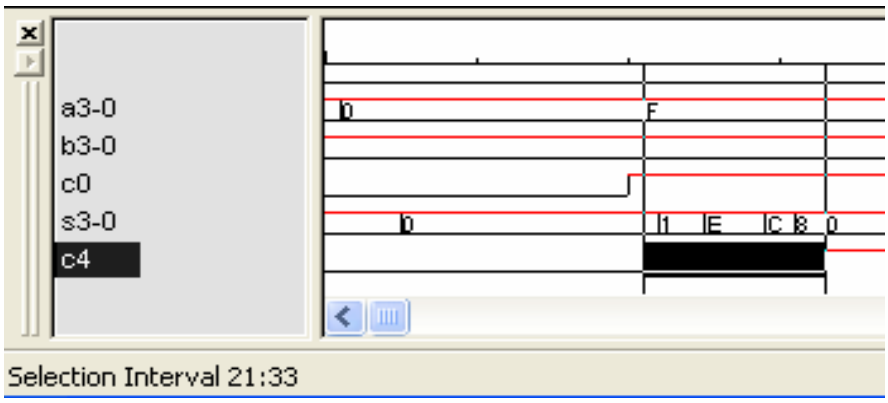


e. Simulate the following values to verify that your adder works properly: 3+4, -1-7, 3+1, 2+5, 3+3.



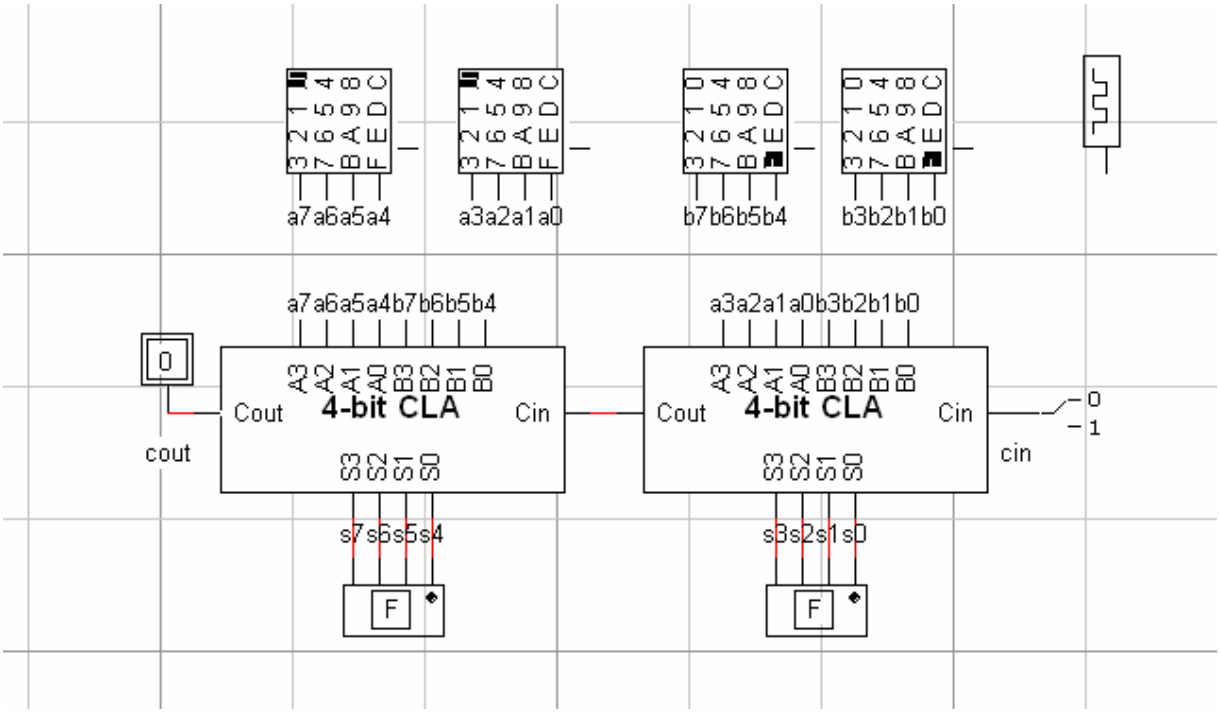
f. Determine the longest delay in the 4-bit Carry Look Ahead adder by simulation.

The longest delay will 2+5+5=12ns. This is as verified by simulation shown below from the time the propagation condition is met until the carry out appears = 33-21=12 ns..



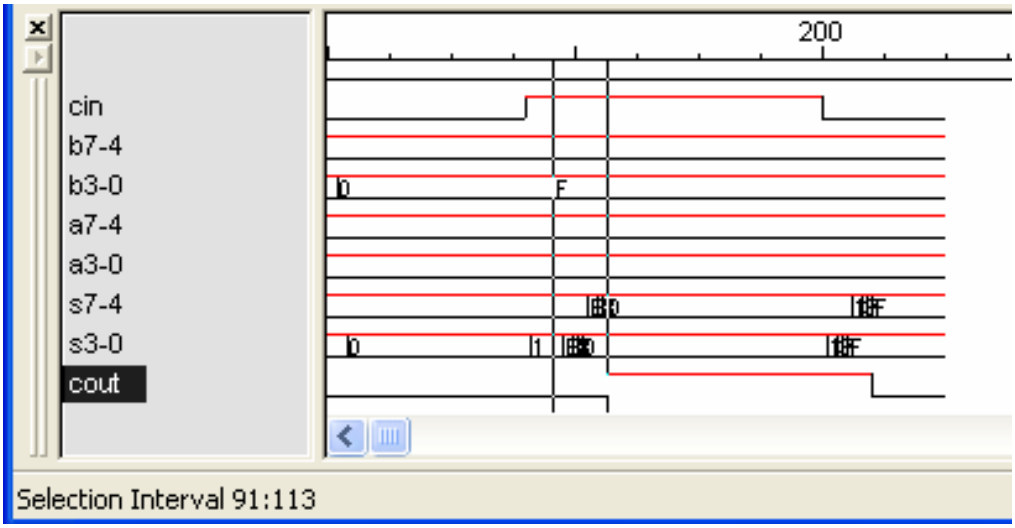
g. Construct an 8-bit adder by connecting two 4-bit Carry Look Ahead adders together.

The 8-bit adder based on two 4-bit CLA adders is shown below:



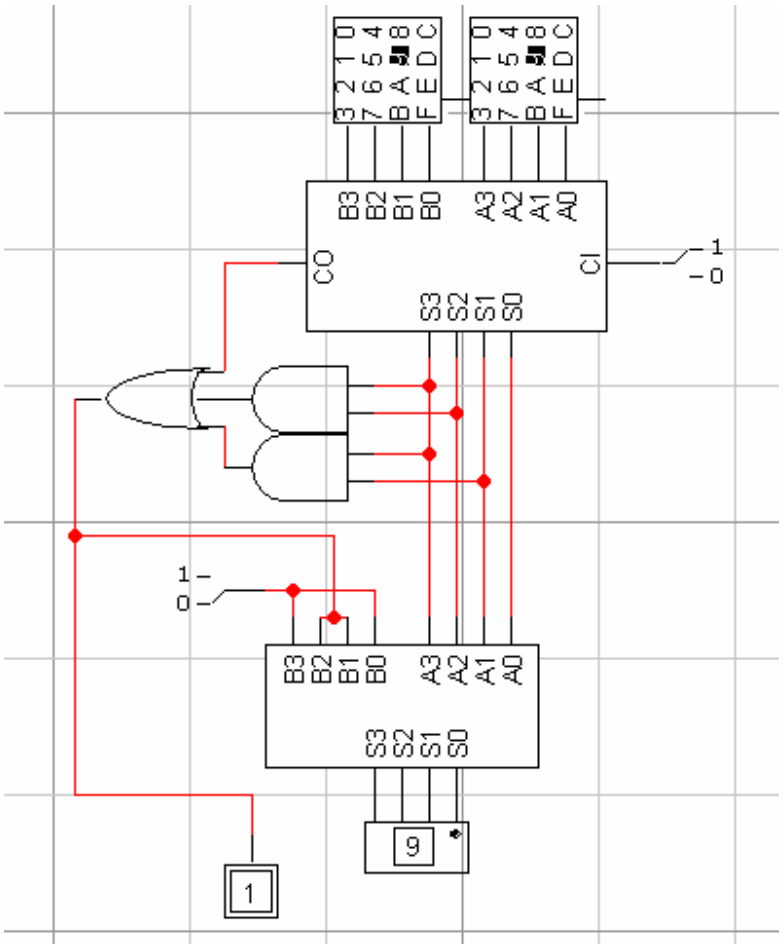
h. Determine by simulation the longest delay in the 8-bit adder in (g).

The worst case delay is 12 (first block) + 10 (2nd block) = 22. This is exactly what is obtained by simulation as shown below = 113-91=22.

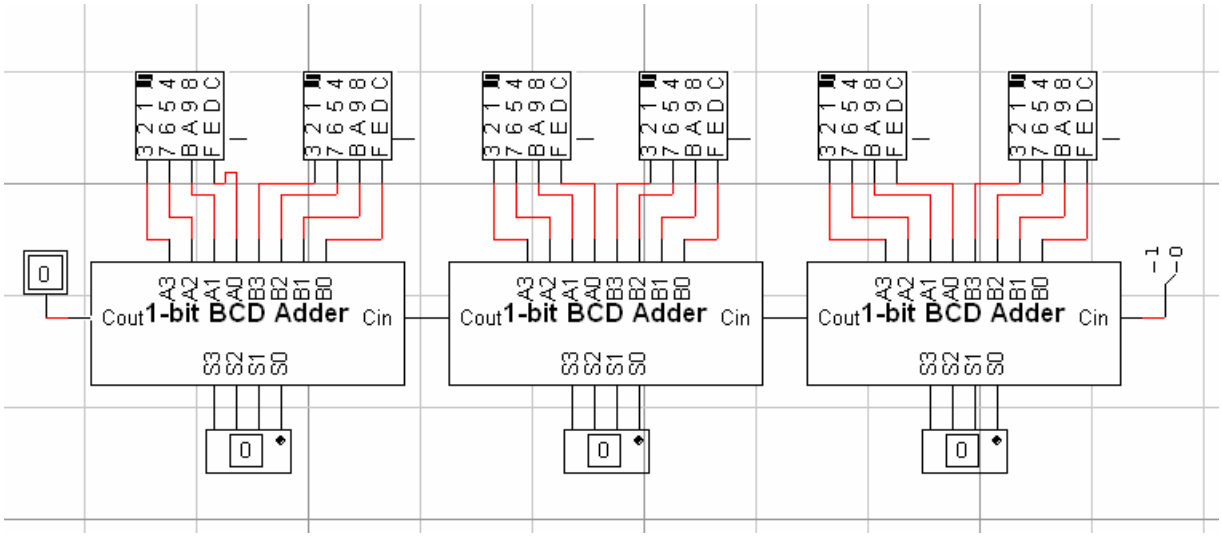


Q.2. It is required to design a BCD adder to perform addition in BCD representation.

a. Model a single-digit BCD adder.

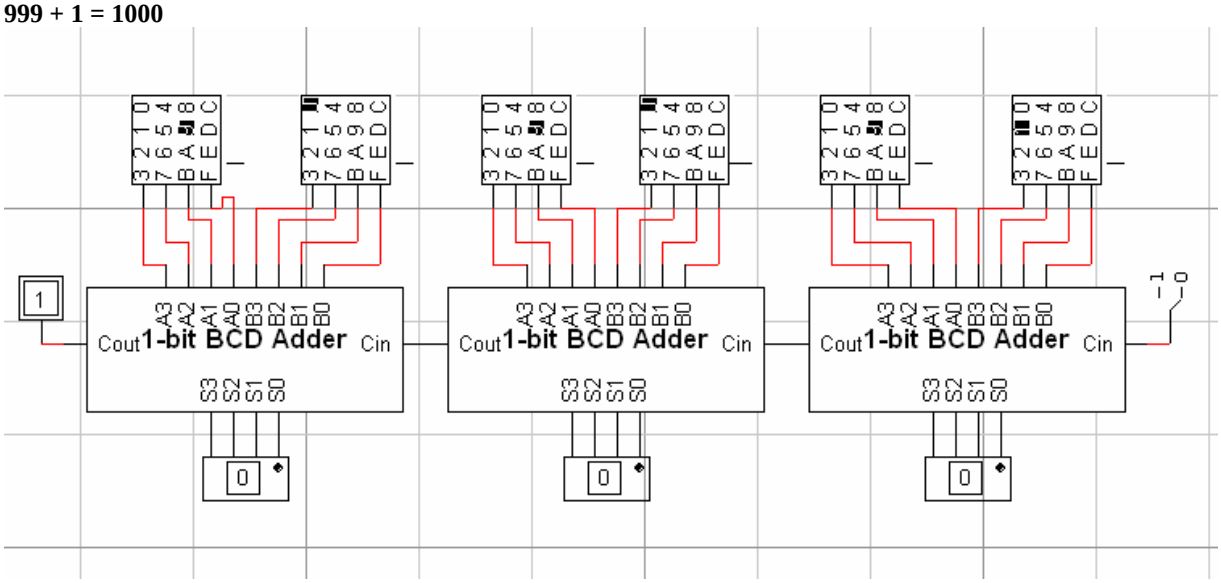


b. Using the single digit BCD adder, build a 3-digit BCD adder.

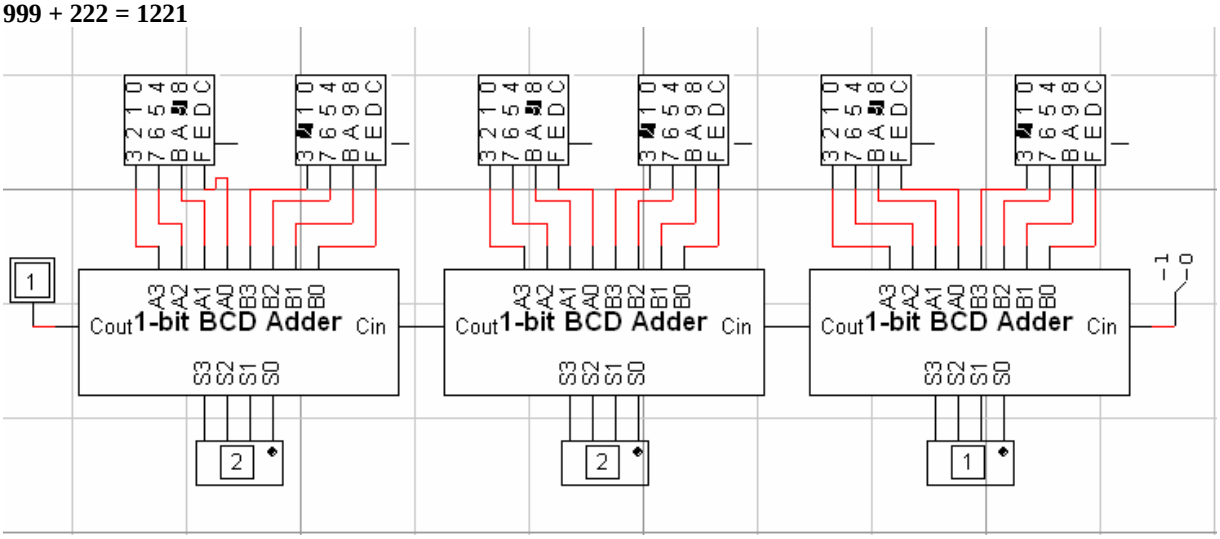


c. Verify the correct functionality of the 3-digit BCD adder by simulating the following operations: 999 + 1, 999+222, 100+999, 279+465

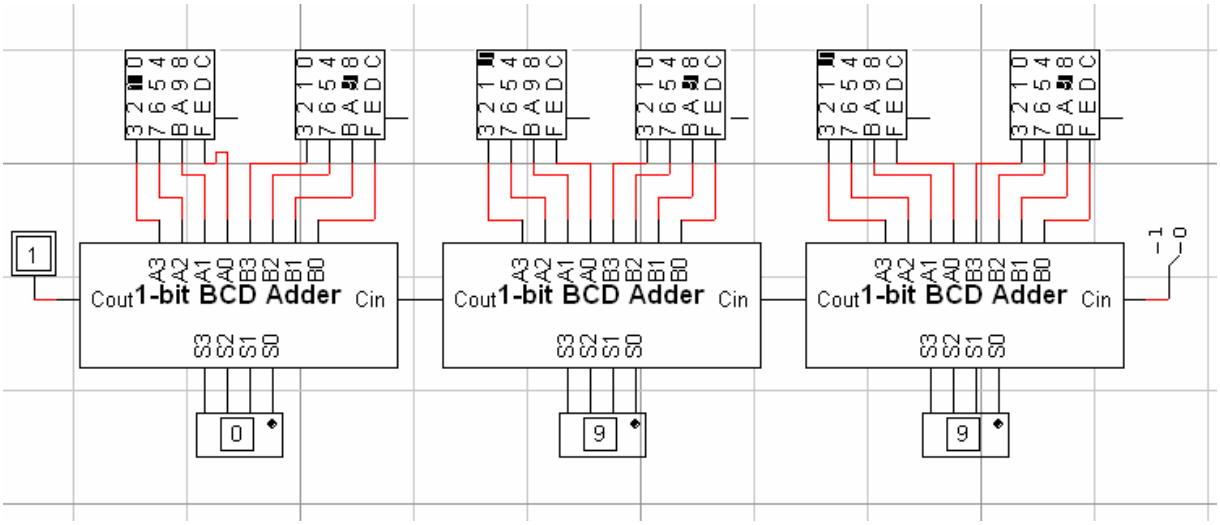
999 + 1 = 1000



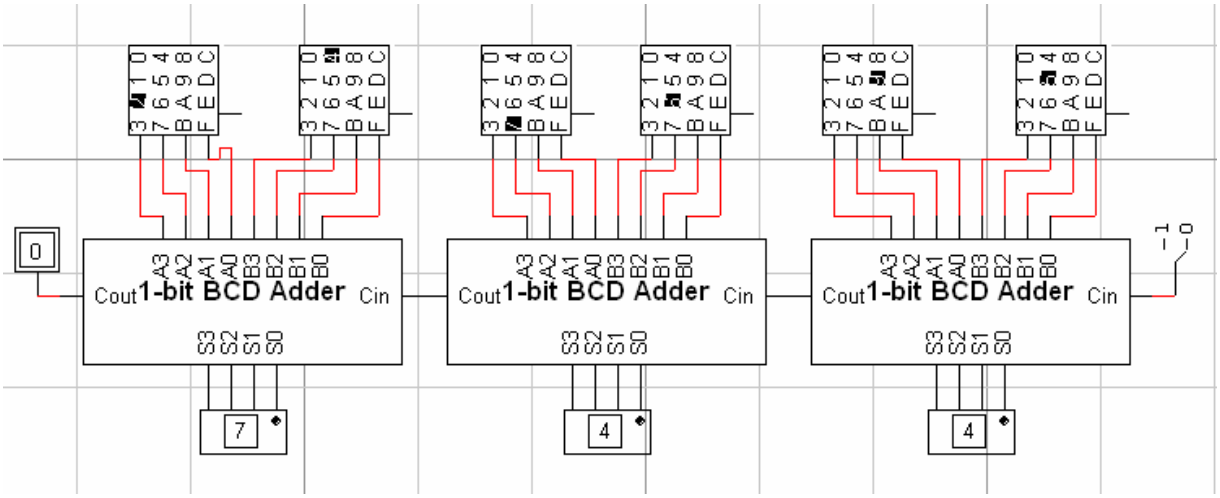
999 + 222 = 1221



100+999 = 1099

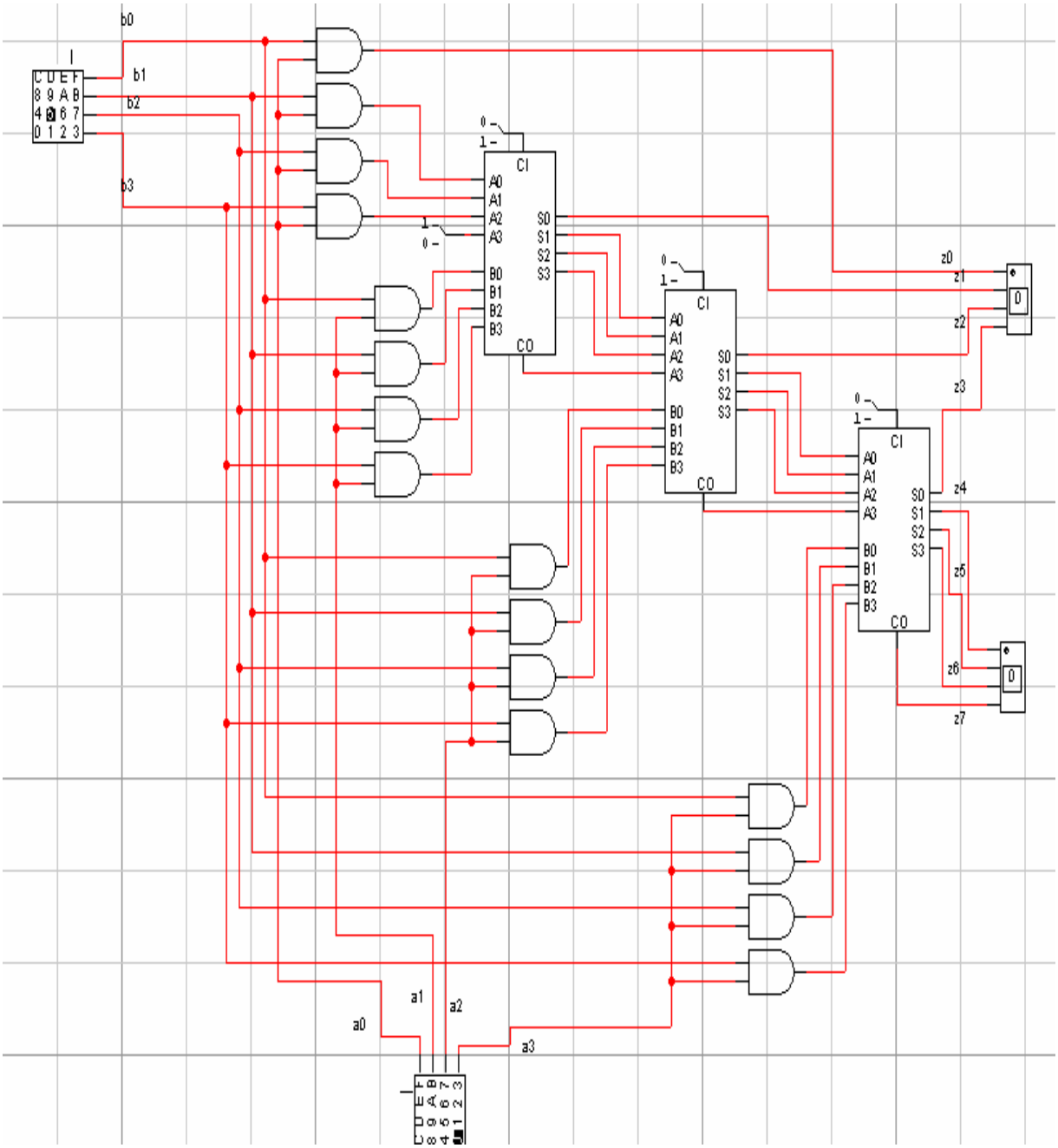


279+465 = 744



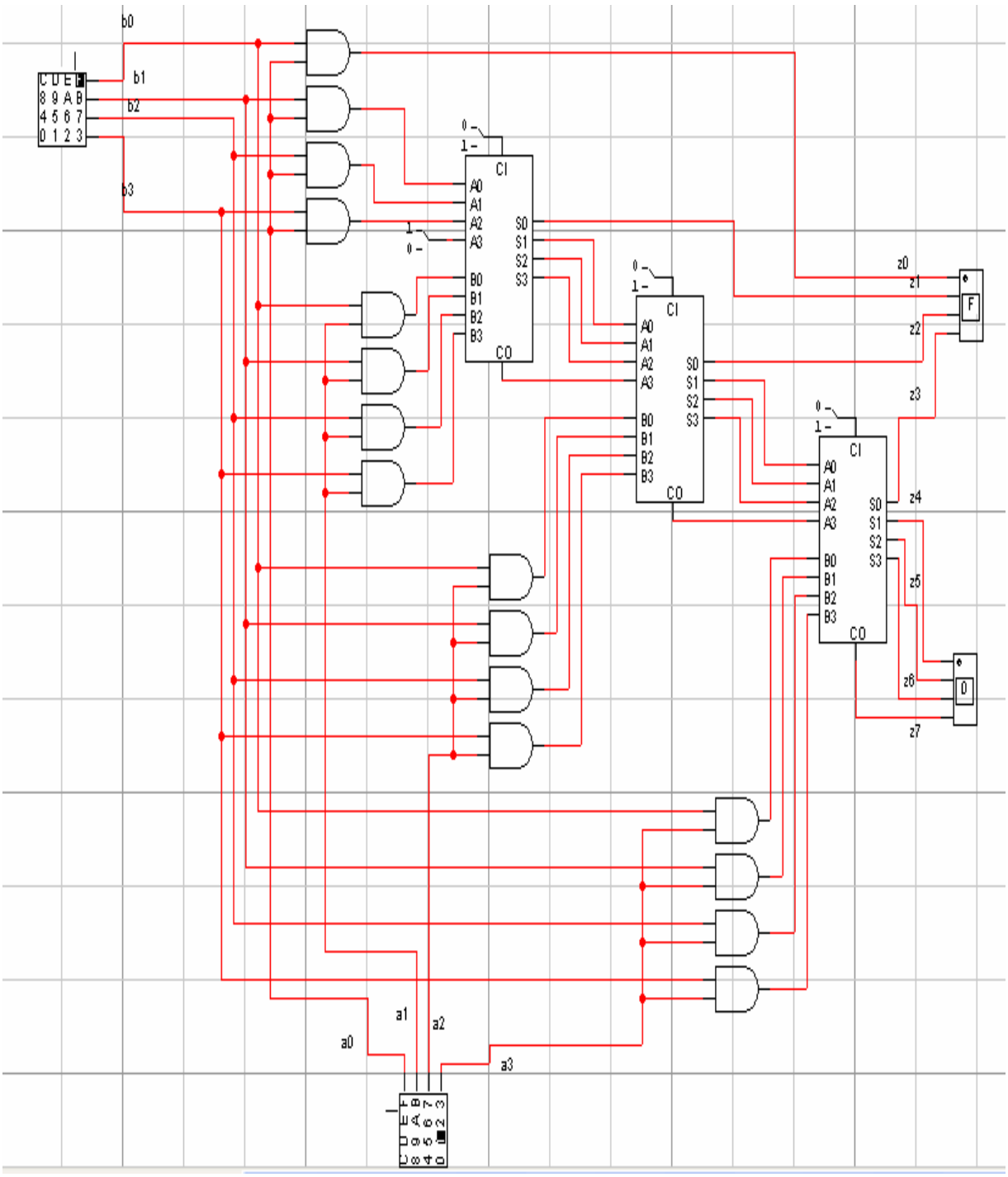
Q.3. [1% Bonus]

a. Model a 4-bit multiplier.

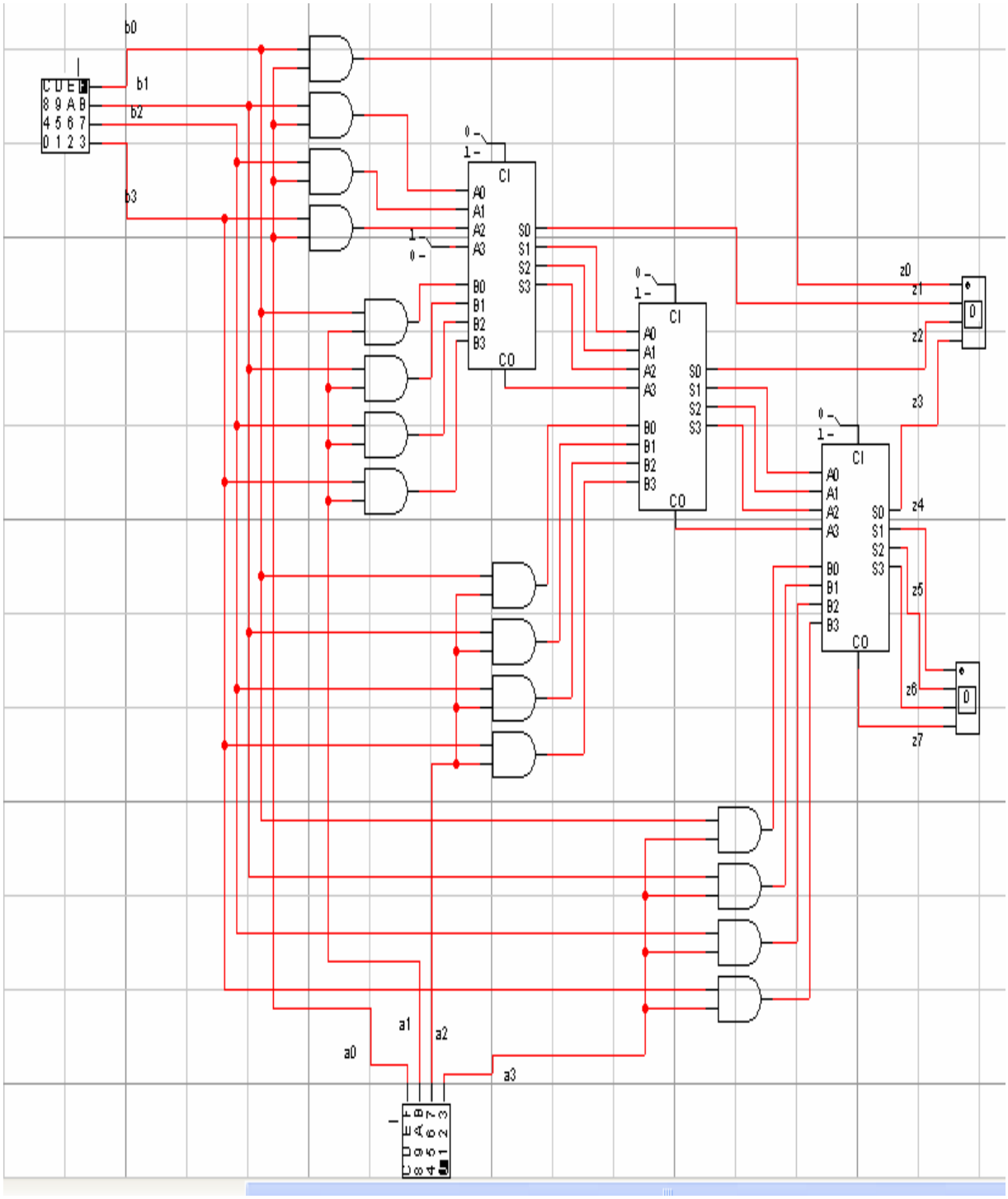


b. Verify the correct functionality of the 4-digit multiplier by simulating the following operations: 15 * 1, 15*0, 5*5, 2*8, 8*7, 15*15.

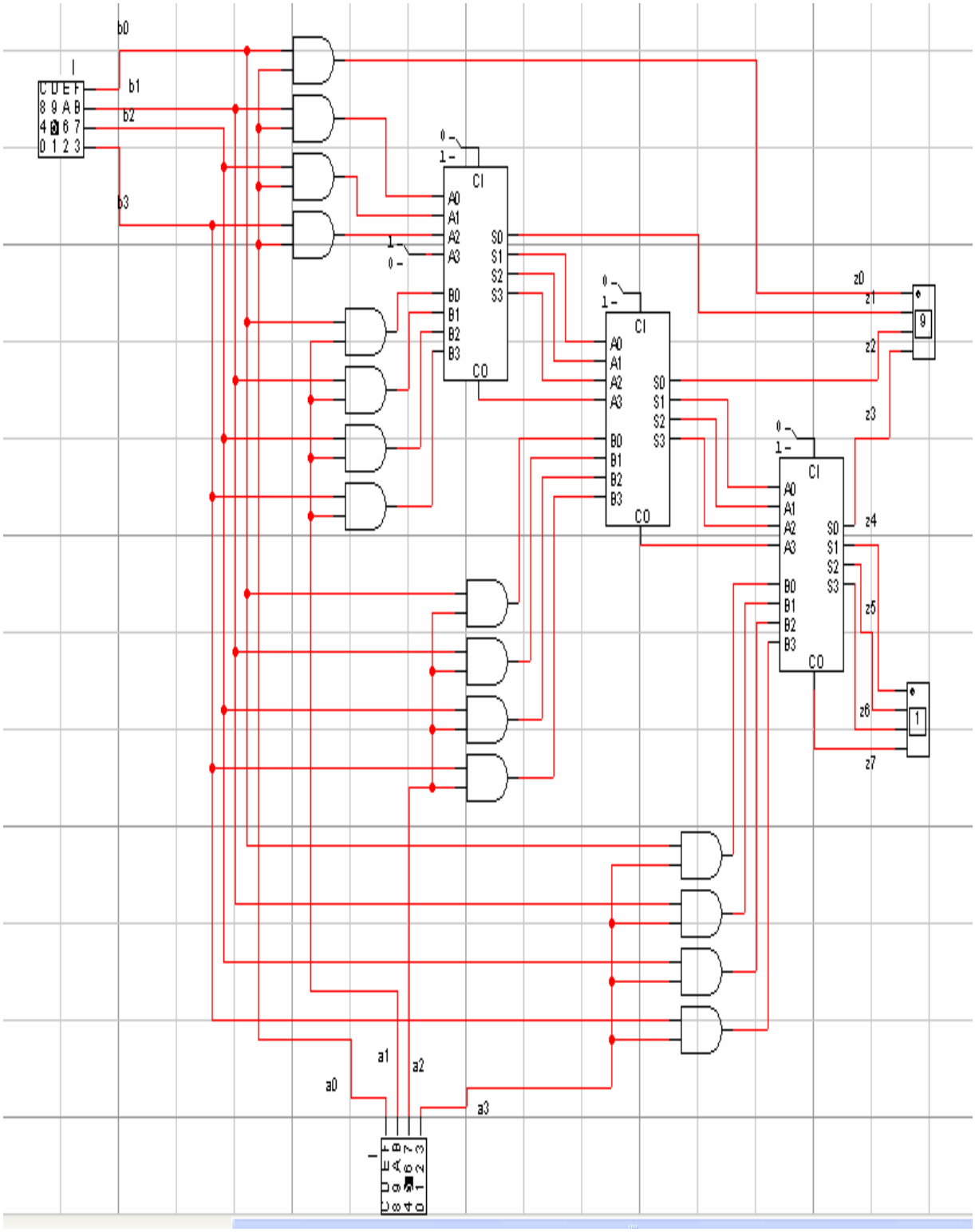
15*1=15=0FH


b0
b1
b2
b3
C D E F
8 9 A B
4 5 6 7
0 1 2 3
CI
A0
A1
A2
A3
B0
B1
B2
B3
S0
S1
S2
S3
CO
z0
z1
z2
z3
z4
z5
z6
z7
F
0
a0
a1
a2
a3

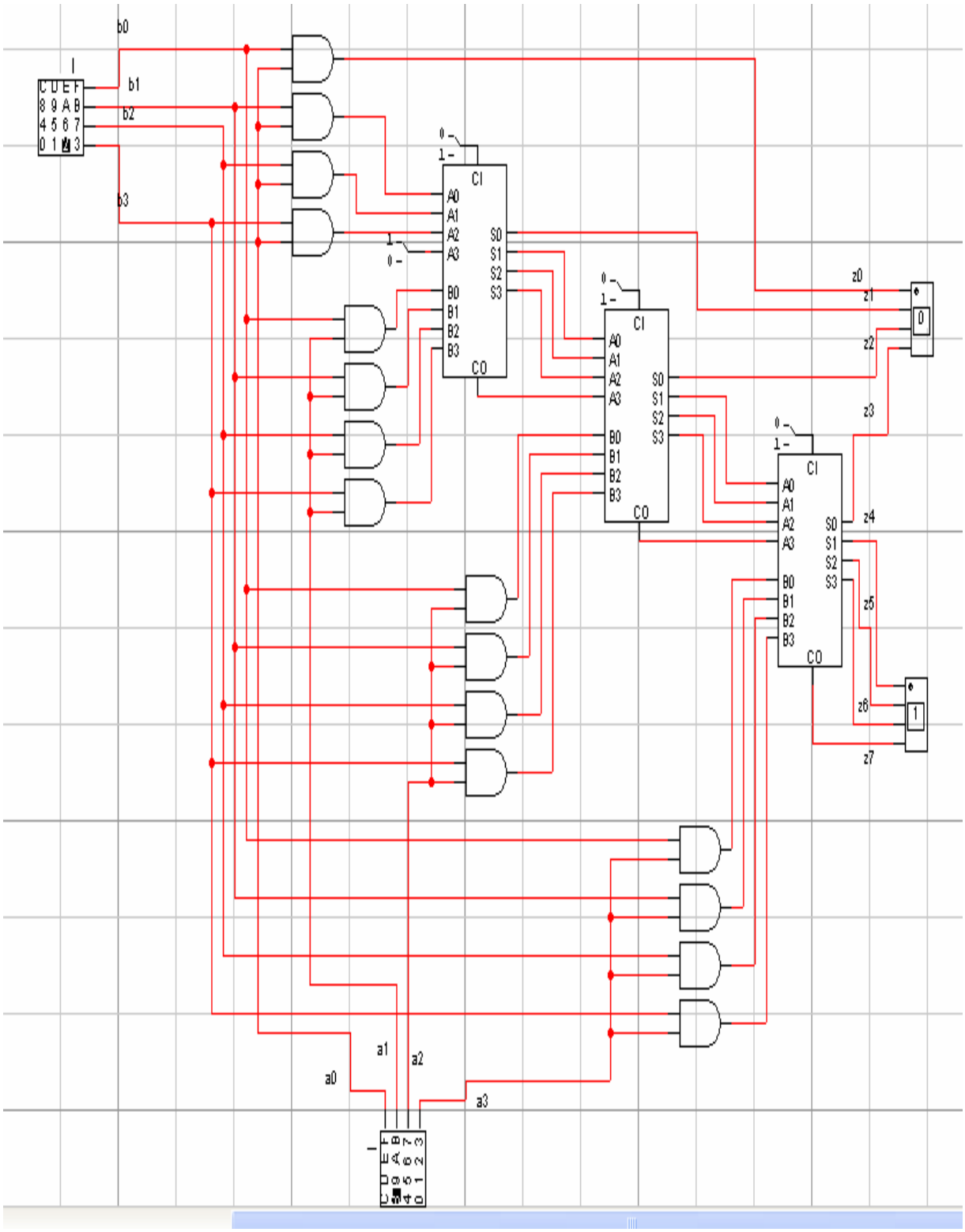
15*0=0


b0
b1
b2
b3
C D E F
8 9 A B
4 5 6 7
0 1 2 3
CI
A0
A1
A2
A3
B0
B1
B2
B3
S0
S1
S2
S3
CO
z0
z1
z2
z3
z4
z5
z6
z7
a0
a1
a2
a3

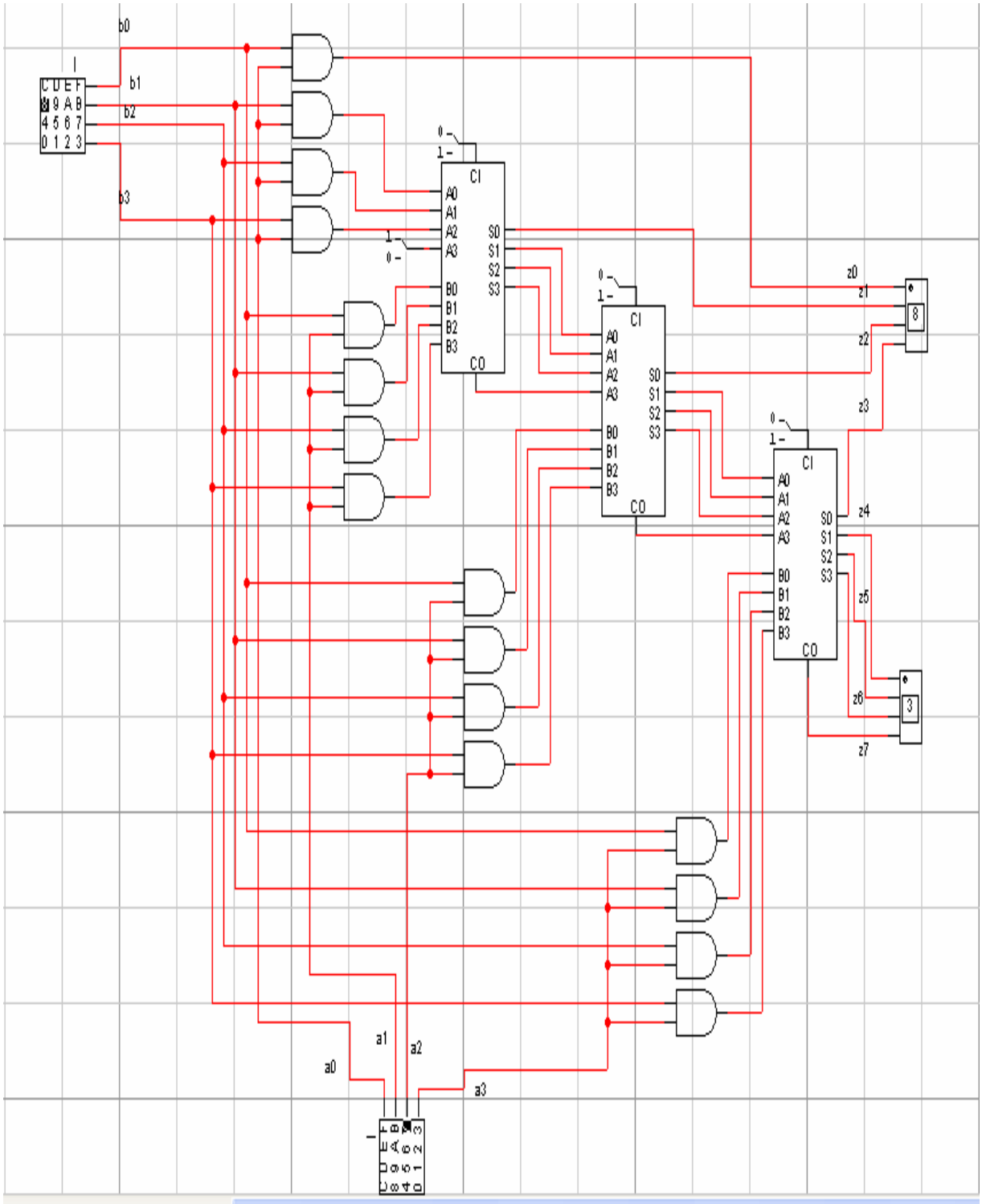
5*5=25=19H


b0
b1
b2
b3
CI
A0
A1
A2
A3
B0
B1
B2
B3
S0
S1
S2
S3
CO
z0
z1
z2
z3
z4
z5
z6
z7
a0
a1
a2
a3

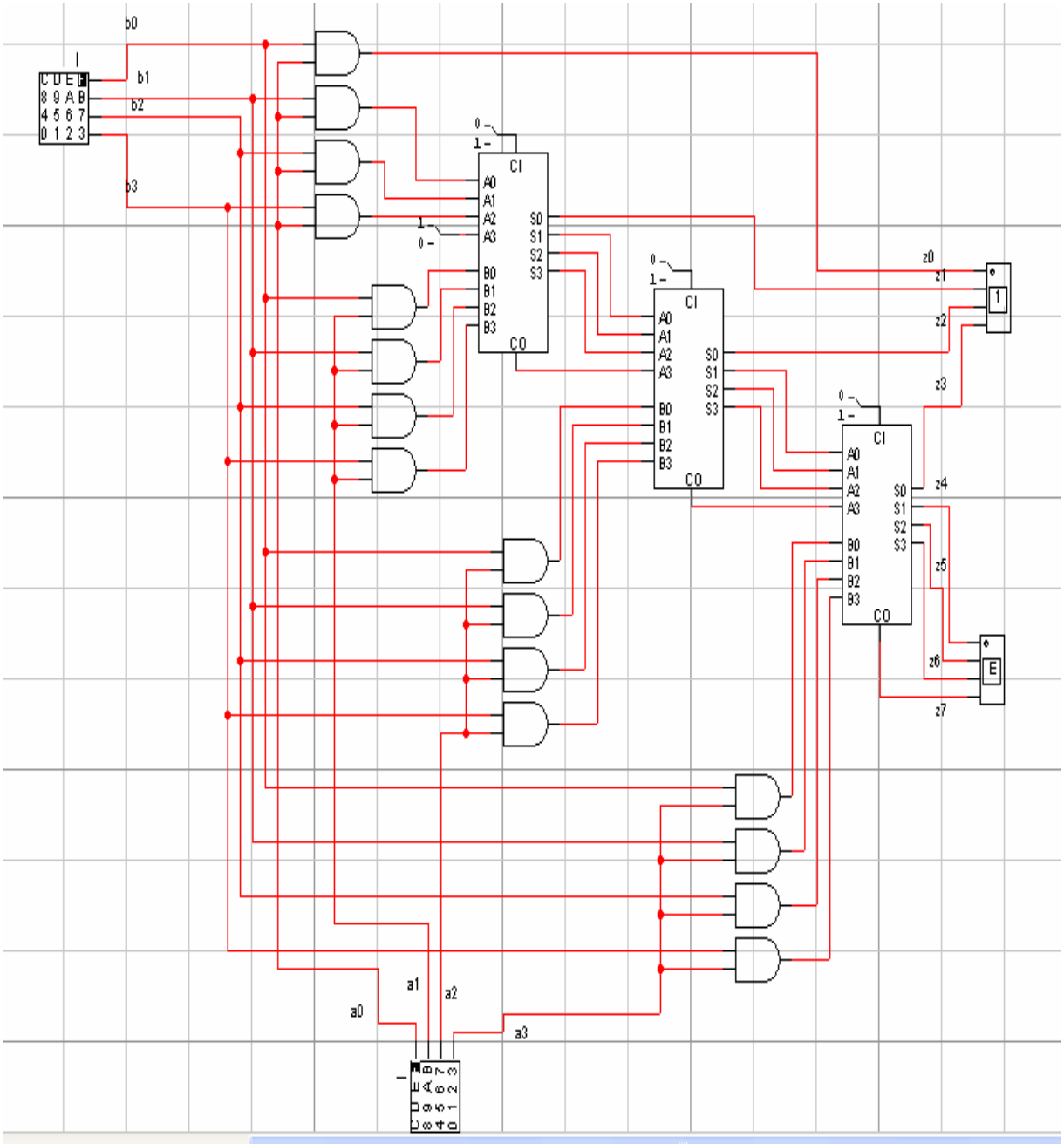
2*8=16=10H


b0
b1
b2
b3
CI
A0
A1
A2
A3
B0
B1
B2
B3
S0
S1
S2
S3
CO
z0
z1
z2
z3
z4
z5
z6
z7
a0
a1
a2
a3

8*7=56=38H


b0
b1
b2
b3
CI
A0
A1
A2
A3
B0
B1
B2
B3
S0
S1
S2
S3
CO
z0
z1
z2
z3
z4
z5
z6
z7
a0
a1
a2
a3

15*15=225=E1H


b0
b1
b2
b3
C D E F
8 9 A B
4 5 6 7
0 1 2 3
CI
A0
A1
A2
A3
B0
B1
B2
B3
S0
S1
S2
S3
CO
z0
z1
z2
z3
z4
z5
z6
z7
1
E
a0
a1
a2
a3