Name: Id#

COE 202, Term 201

Digital Logic Design

Quiz# 5

 Date: Sunday, Nov. 8, 2020

**Question 1: (9 points)**

Given an n-bit signed 2's complement number, **X**,it is required to design an iterative combinational circuit to compute the 2's complement of **X**.

1. Sow the inputs and outputs of the 1-bit 2's complement iterative cell to be used for designing the n-bit 2's complement circuit. (2 Points)
2. Show the truth table of the 1-bit 2's complement cell. (4 Points)
3. Obtain simplified equations for the outputs of the 1-bit 2's complement cell using only the following gate types: NOT, AND, OR, XOR. (2 Points)
4. Using the 1-bit 2's complement cell, draw a block diagram for a circuit to compute the 2's complement of a 3-bit number X. (1 Point)

**Question 2. (14 Points)**

1. Fill in all blank cells in the two tables below.

|  |  |
| --- | --- |
| Binary | Equivalent decimal value with the binary interpreted as: |
| Unsigned number | Signed-magnitude number | Signed-1’s complement number  | Signed-2’s complement number |
| 1011 1010 |  |  |  |  |

|  |  |
| --- | --- |
| Decimal | Binary representation in 8 bits: |
| Signed-magnitude representation | Signed-1’s complement representation  | Signed-2’s complement representation |
| + 90 |  |  |  |
|  - 90 |  |  |  |

1. Show how the following arithmetic operations are performed using 5-bit signed 2’s-complement system. Check for overflow and mark clearly any overflow occurrences.

|  |  |
| --- | --- |
| (i) 01101 - 11100 Overflow: Yes/No |  (ii) 10010 + 11110   Overflow: Yes/No |
| (iii) 11111 + 11111   Overflow: Yes/No |  (iv) 01011 - 11011  Overflow: Yes/No |