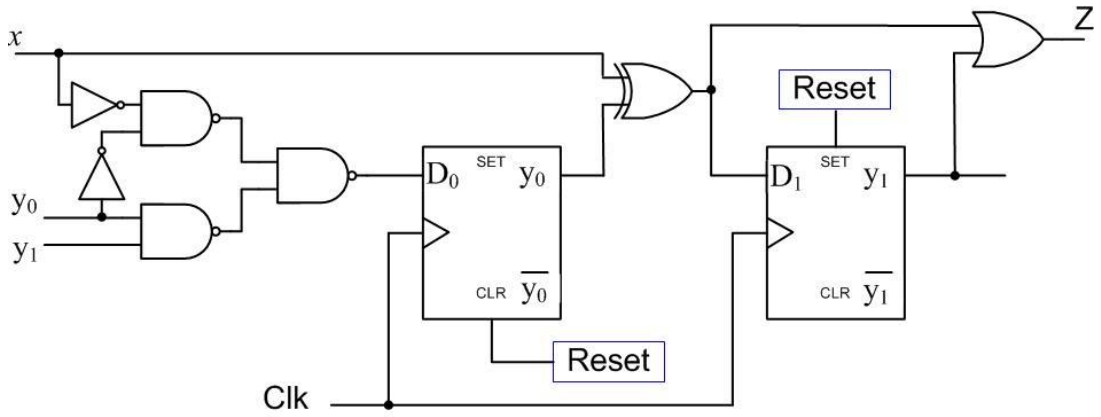
Name: **Id#**

COE 202, Term 151
Digital Logic Design

Quiz# 5

Date: Thursday, Dec. 10

Q1. The sequential circuit shown below has a single output Z, an input *x* together with a Reset input to initialize the circuit. Note that the used D-FFs have direct/asynchronous Clear and Set inputs (shown in the figure as CLR and SET).



a. Is the circuit type Mealy or Moore? Why?

b. Derive expressions for the D_0 and D_1 flip flop inputs and the external output Z.

c. Derive the state transition table of the circuit.

d. What is the circuit initial state?

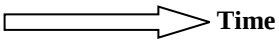
Q2. Consider the following state transition table for a synchronous sequential circuit that multiplies a binary number by 3 i.e. Z=3*X. The circuit has a single input **X**, a single output **Z**, and two state variables $\mathbf{Y_0}$, and $\mathbf{Y_1}$. The states are encoded using binary codes **00**, **01**, **10.**

PS $(Y_1\ Y_0)^t$	**NS** $(Y1\ Y_0)^{t+1}$		**Z**	
	X = 0	**X = 1**	**X = 0**	**X = 1**
0 0	0 0	0 1	0	1
0 1	0 0	1 0	1	0
1 0	0 1	1 0	0	1

Using D-FFs and minimal combinational logic, determine the equations for the D-FF inputs and the output Z for this circuit and draw the resulting circuit. State 00 is the reset state.

Q3. It is required to design a synchronous sequential circuit that receives a serial sequence of **3-bit codes** through input **X** and produces **1** through output **Y** when the received 3-bit code equals either 010 or 110 (i.e., either 0 followed by 1 followed by 0, or 1 followed by 1 followed by 0). Assume the availability of an asynchronous reset input to reset the machine to a reset state. Draw the state diagram of the circuit assuming a **Mealy** model with **minimum** number of states. *You are not required to derive the equations and the circuit.* The following is an example of an input and output sequence:

Example:



Input	**X**	0 1 0 0 0 1 0 0 1 1 0 1 1 1 0
Output	**Y**	0 0 1 0 0 0 0 0 0 0 0 0 0 0 1