Name: **Id#**

COE 202, Term 131
Digital Logic Design

Quiz# 5

Date: Thursday, Nov. 28

Q1. Fill in all blank cells in the two tables below. All binary representations use 7 bits

Binary	Equivalent decimal value with the binary interpreted as:			
	Unsigned number	Signed-magnitude number	Signed-1's complement number	Signed-2's complement number
1011010				

Decimal	Binary representation in:		
	Signed-magnitude notation	Signed-1's complement notation	Signed-2's complement notation
- 59			

b. Using 2's-complement signed arithmetic in **5 bits**, perform the following operations in binary. Show all your work. Verify that you get the expected decimal results.
Check for overflow and mark clearly any occurrences of it.

(i) 11010 + 11001	(ii) 00101 - 10100
(iii) (+5) + (-9)	(iv) (-6) - (+8)

c. When doing signed 2's complement arithmetic in **6 bit**s, the *smallest* binary number **that will cause overflow** when *subtracted* from $(101000)_2$ is _____.

Q2.

(a) You are given **one 3-to-8 decoder**, **one NOR** gate and **one OR** gate to implement the two functions given below.

$$F_1(A,B,C) = \Pi M(0, 1, 4, 5, 6)$$
$$F_2(A,B,C) = \sum m(0, 4, 6) + \sum d(1, 3)$$

Draw the circuit and properly label all input and output lines.

(b) Given the truth table below for a function with four inputs (A, B, C and D) and one output F, implement F using a 4-to-1 MUX (with 2 select lines) and additional logic. Show how you obtained your solution, and properly label all input and output lines. Apply A and B to the select inputs.

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0