Name: **Id#**

COE 202, Term 122
Digital Logic Design

Quiz# 5

Date: Monday, April 29

Q1.

(i) Design a D-Latch using only NAND gates.

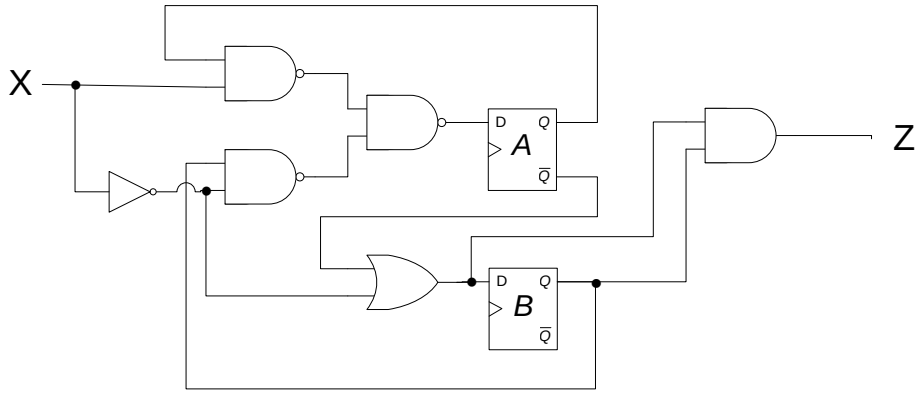
(ii) Design a D-Latch using only a 2x1 Multiplexer.

(iii) Design a **rising-edge** triggered D flip flop using only D-Latches and inverters.

Q2. Design a **falling-edge** triggered JK flip flop using a **rising-edge** triggered D flip flop. Show the design steps.

Q3.

(i) Derive the state table and state diagram for the following circuit with a single input X, and a single output Z and determine whether the circuit is Mealy or Moore:



(ii) Complete the following waveform for the positive-edge triggered circuit that implements the state diagram provided below. Assume the circuit is initially at the state $Q_1Q_0 = 00$.