Name: **Id#**

COE 202, Term 112
Digital Logic Design

Quiz# 5

Date: Wednesday, April 25

Q1. Design a rising edge-triggered D flip-flop using a rising edge-triggered JK flip flop.

Q2. A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following equations:

$$D_A = X` Y + X A \qquad D_B = X` B + X A \qquad Z = B$$

(i) Draw the logic diagram of the circuit.

(ii) Derive the state table.

(iii) Derive the state diagram.