Name: **Id#**

COE 202, Term 052
Fundamentals of Computer Engineering

Quiz# 5 (Take Home)

Due date: Monday, April 17, 2006

Q.1. Assume the delay of a gate is equal to the number of its inputs, i.e. the delay of a 2-input gate is 2, and the delay of a 3-input gate is 3. Using Logic works do the following:

a. Model a full-adder.
b. Use the full adder model and construction from it an 8-bit Ripple Carry Adder.
c. Determine the worst case delay in your 8-bit Ripple Carry Adder by simulation.
d. Model a 4-bit Carry Look Ahead adder.
e. Simulate the following values to verify that your adder works properly: 3+4, -1-7, 3+1, 2+5, 3+3.
f. Determine the longest delay in the 4-bit Carry Look Ahead adder by simulation.
g. Construct an 8-bit adder by connection two 4-bit Carry Look Ahead adders together.
h. Determine by simulation the longest delay in the 8-bit adder in (g).

Q.2. It is required to design a BCD adder to perform addition in BCD representation.

a. Model a single-digit BCD adder.
b. Using the single digit BCD adder, build a 3-digit BCD adder.
c. Verify the correct functionality of the 3-digit BCD adder by simulating the following operations: 999 + 1, 999+222, 100+999, 279+465

Q.3. [1% Bonus]

a. Model a 4-bit multiplier.
b. Verify the correct functionality of the 4-digit multiplier by simulating the following operations: 15 * 1, 15*0, 5*5, 2*8, 8*7, 15*15.