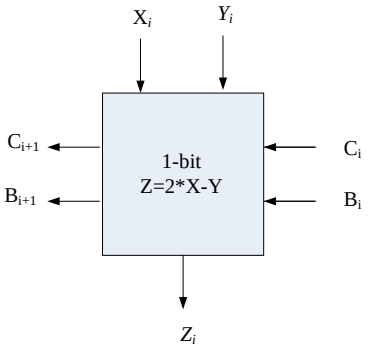
Name: KEY **Id#**

COE 202, Term 141
Digital Logic Design

Quiz# 4

Date: Thursday, Nov. 20

Q1 It is required to design a circuit to compute the equation Z=2*X-Y, where X and Y are two n-bit unsigned numbers. The circuit can be designed in a modular manner where it is designed for one bit and replicated *n* times. A 1-bit circuit block diagram is given below:

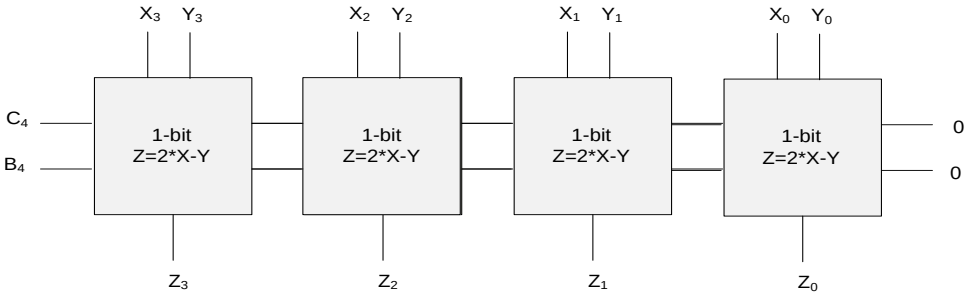


The meaning of the values of B_i and C_i is given in the table below:

B_i	C_i	Meaning
0	0	There is no carry or borrow
0	1	There is a carry of 1
1	0	There is a borrow of 1
1	1	This condition does not occur

For example, if X_i=1 and Y_i=1, then we should have Z_i=1, B_{i+1}=0 and C_{i+1}=0. If X_i=0 and Y_i=1, then we should have Z_i=1, B_{i+1}=1 and C_{i+1}=0.

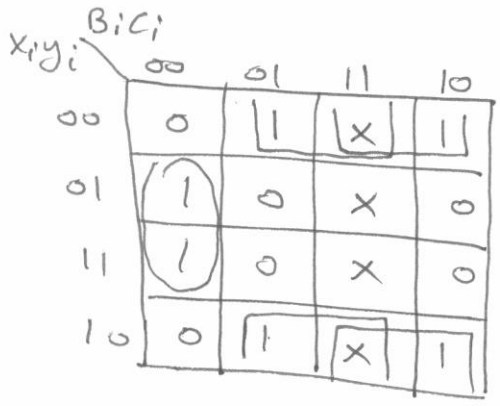
The figure below shows how a 4-bit Z=2*X-Y circuit is implemented using 4 copies of the basic 1-bit cell.



Derive the truth table for the basic one-bit cell. Derive the equation for the Z output only.

Truth Table:

X_i	Y_i	B_i	C_i	B_{i+1}	C_{i+1}	Z_i
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	1	0	1
0	0	1	1	X	X	X
0	1	0	0	1	0	1
0	1	0	1	0	0	0
0	1	1	0	1	0	0
0	1	1	1	X	X	X
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	0	0	1
1	0	1	1	X	X	X
1	1	0	0	0	0	1
1	1	0	1	0	1	0
1	1	1	0	0	0	0
1	1	1	1	X	X	X



$$Z_i = \bar{y_i} C_i + \bar{y_i} B_i + y_i \bar{B_i} \bar{C_i}$$

$$= \bar{y_i} (B_i + C_i) + y_i \overline{(B_i + C_i)}$$

$$= y_i \oplus (B_i + C_i)$$