Name: KEY Id#

COE 202, Term 141

Digital Logic Design

Quiz# 4

 Date: Thursday, Nov. 20

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**Q1**  It is required to design a circuit to compute the equation Z=2\*X-Y, where X and Y are two n-bit unsigned numbers. The circuit can be designed in a modular manner where it is designed for one bit and replicated *n* times. A 1-bit circuit block diagram is given below:



The meaning of the values of Bi and Ci is given in the table below:

|  |  |  |
| --- | --- | --- |
| Bi | Ci | Meaning |
| 0 | 0 | There is no carry or borrow |
| 0 | 1 | There is a carry of 1 |
| 1 | 0 | There is a borrow of 1 |
| 1 | 1 | This condition does not occur |

For example, if Xi=1 and Yi=1, then we should have Zi=1, Bi+1=0 and Ci+1=0. If Xi=0 and Yi=1, then we should have Zi=1, Bi+1=1 and Ci+1=0.

# The figure below shows how a 4-bit Z=2\*X-Y circuit is implemented using 4 copies of the basic 1-bit cell.



# Derive the truth table for the basic one-bit cell. Derive the equation for the Z output only.

**Truth Table**:

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Xi | Yi | Bi | Ci | Bi+1 | Ci+1 | Zi |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | X | X | X |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | X | X | X |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | X | X | X |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | X | X | X |

