Name: KEY **Id#**

COE 202, Term 132
Digital Logic Design

Quiz# 4

Date: Tuesday, April 15

Q1. Determine the decimal value of the 7-bit binary number (1011010) when interpreted as:

An unsigned number	A signed-magnitude number	A signed-1's complement number	A signed-2's complement number
90	−26	−37	−38

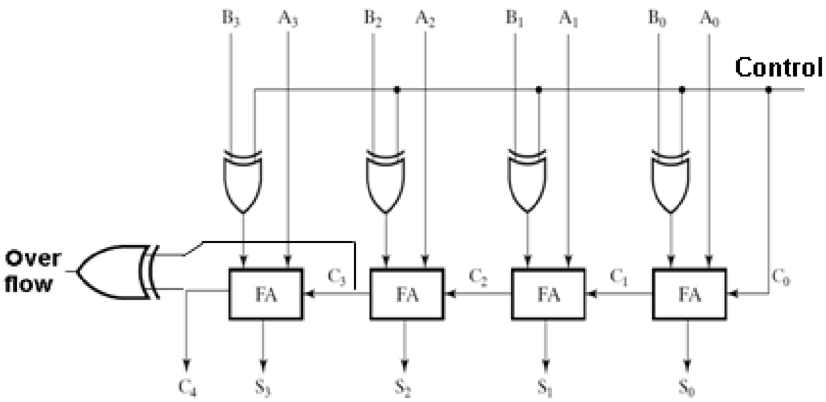
ii. Represent the decimal value (- 21) in binary using a total of 7 bits in the following notations:

A signed-magnitude number	A signed-1's complement number	A signed-2's complement number
1010101	1101010	1101011

iii. Perform the following signed-2's complement arithmetic operations in binary using 5 bits. All numbers given are represented in the signed-2's complement notation. Indicate clearly the carry values from the last two stages. For each of the three operations, check and indicate whether overflow occurred or not.

01010	1←1←1← a. 01101 +13 +10110 + −10 00011 +3 ✓	b. 01010 +10 - 11001 00111 −(−7) +17 0←1←1←1← 01010 +00111 10001 ~~−15~~	c. 11010 00110 −6 - 00100 − +4 −10 1←1← 11010 +11100 10110 = − 01010 = −10 ✓
Overflow Occurred? (Yes/No)	No	Yes	NO

(B) Consider the 2's complement 4-bit adder/subtractor hardware shown (**FA** = full adder).



i. Fill in the spaces in the table below.

Inputs			Outputs			
A	**B**	Control	S (binary)	C_4	C_3	Overflow
0111	0101	0	1100	0	1	1
1010	1101	1	1101	0	0	0

0 ← 1 ← 1 ← 1 ←
0111
+0101
1100

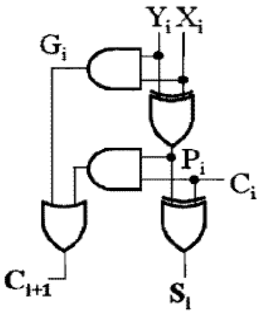
0 ← 0 ← 1 ←
1010 → 1010
−1101 → +0011
1101

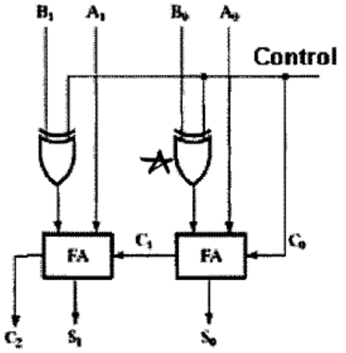
ii. What type of 4-bit adder is used in this design? (Circle the correct answer):

[✓ - Carry-ripple adder]
- Carry-look-ahead adder

b. Consider a 2-bit version of the hardware above which is shown below. Shown also is full adder used. Given that each basic gate (i.e. AND, OR, NOT) has a delay of τ ns and the XOR gate has a delay of 3τ:

The Full Adder (FA)





i. Express, as a function of τ, the longest time interval needed for the hardware to perform an operation on the two 2-bit numbers.

$(\overset{\star}{3} + 3 + 2 + 3)\tau = 11\tau$

ii. If such an operation must be performed in no longer than 33 ns, calculate the maximum basic gate delay allowed.

33 ns / 11 = 3 ns