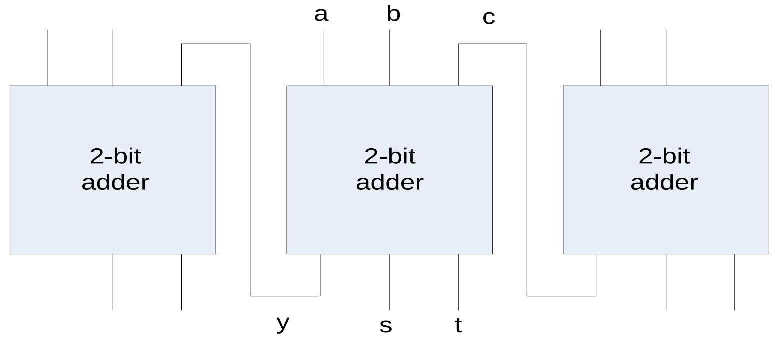
Name: KEY **Id#**

COE 202, Term 122
Digital Logic Design

Quiz# 4

Date: Monday, April 8

Q1. We would like to design an adder to add the 8-bit constant 10101010 to an arbitrary 8-bit number. The adder is to be designed using four identical adder modules, each of which will add 2 bits of the number to the constant (10) and a carry from the next lower pair of bits and produce 2 bits of the sum and the carry to the next bits. A block diagram of part of this design is shown below:



The problem each 2-bit adder solves is:

$$\begin{array}{cccc} & & & c \\ & & a & b \\ + & & 1 & 0 \\ \hline & y & s & t \end{array}$$

(i) Show a truth table for the 2-bit adder (it has three inputs: a, b, and c, and it has three outputs: y, s, and t), and find minimal SOP expressions for each output.

(ii) Compute the delay from the c-input of each module to the y output of that module and the total delay for the 8 bits. Assume that the delay of a gate is related to the number of inputs i.e. the delay of an inverter is 1, the delay of a 2-input gate is 2, etc.

(i)

a	b	c	y	s	t
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	0	1
1	1	1	1	1	0

a \ bc	00	01	11	10
0	0	0	1	0
1	1	1	1	1

$y = a + bc$

a \ bc	00	01	11	10
0	1	1	0	1
1	0	0	1	0

$s = \bar{a}\bar{b} + \bar{a}\bar{c} + abc$

a \ bc	00	01	11	10
0	0	1	0	1
1	0	1	0	1

$t = \bar{b}c + b\bar{c}$

(ii) Delay from the c-input of each module to the y-output of the module = 2 + 2 = 4

Since the first block does not have a carry in, a carry is generated when a = 1. Thus, the delay of y = 2.

For the 2nd block & 3rd block, each will add a delay of 4. Thus, the delay of the carry out of the 3rd block is 2 + 4 + 4 = 10

For the 4th block, the delay across the s output is the largest which is 10 + 3 + 3 = 16. Thus, the longest delay across the circuit is 16.

Q2.

(i) Determine the decimal value of the 7-bit binary number (1011010) when interpreted as:

An unsigned number	A signed-magnitude number	A signed-1's complement number	A signed-2's complement number
90	-26	-37	-38

(ii) Represent the decimal value (- 21) in binary <u>using a total of 7 bits</u> in the following notations:

A signed-magnitude number	A signed-1's complement number	A signed-2's complement number
1010101	110 1010	11 01011

(iii) Perform the following signed-2's complement arithmetic operations in binary using 5 bits. All numbers given are represented in the signed-2's complement notation. Indicate clearly the <u>carry values from the last two stages</u>. For each of the three operations, check and indicate whether overflow occurred or not.

	11 a. 01101 +10110 100011	b. 01010 - 11001 111 01010 +00111 010001	c. 11010 - 00100 1 11010 +11100 1 10110
Overflow Occurred? (Yes/No)	NO	Yes	No