Name: KEY **Id#**

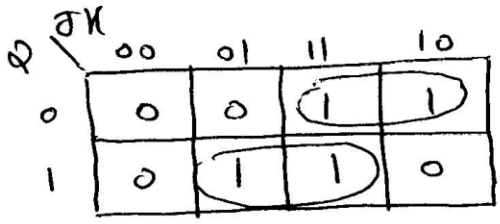
COE 202, Term 121
Digital Logic Design

Quiz# 4

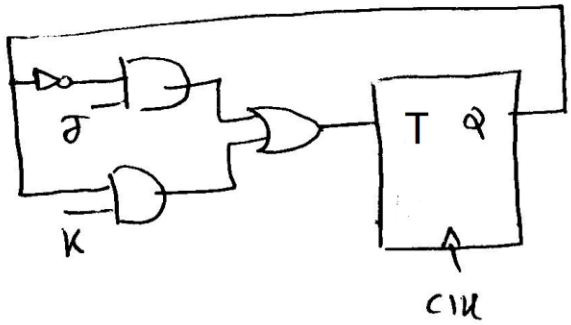
Date: Monday, Dec. 10

Q1. Design a JK flip flop using a T flip flop.

Q	J	K	Q^+	T
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1



$$T = \bar{Q}J + QK$$



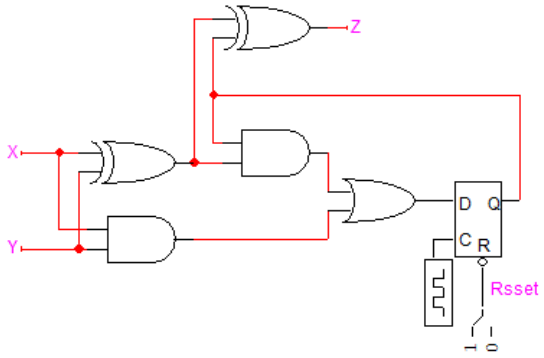
Q2. Given the following synchronous sequential circuit with two inputs {X, Y} and one output {Z}:

(i) Derive the state table of the circuit.

(ii) Show the state diagram of the circuit.

(iii) Is the circuit Mealy or Moore?

(iv) Determine the output sequence for the input sequence XY={00, 01, 10, 11, 00}. Note that 00 is the start of the sequence. Assume that the machine is reset to the state 0.



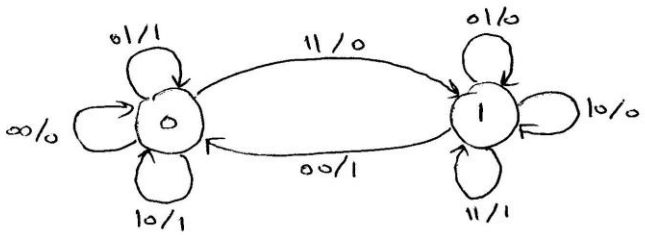
(i) $Z = x \oplus y \oplus Q$

$D = xy + Q(x \oplus y)$

State Table:

Q	x	y	Q^+	Z
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(ii) State Diagram:



(iii) The circuit is Mealy because the output Z depends on the inputs and current state Q.

(iv) $0 \xrightarrow[0]{00} 0 \xrightarrow[1]{01} 0 \xrightarrow[1]{10} 0 \xrightarrow[0]{11} 1 \xrightarrow[1]{00} 0$

Thus, the output sequence produced is $\{0, 1, 1, 0, 1\}$.