

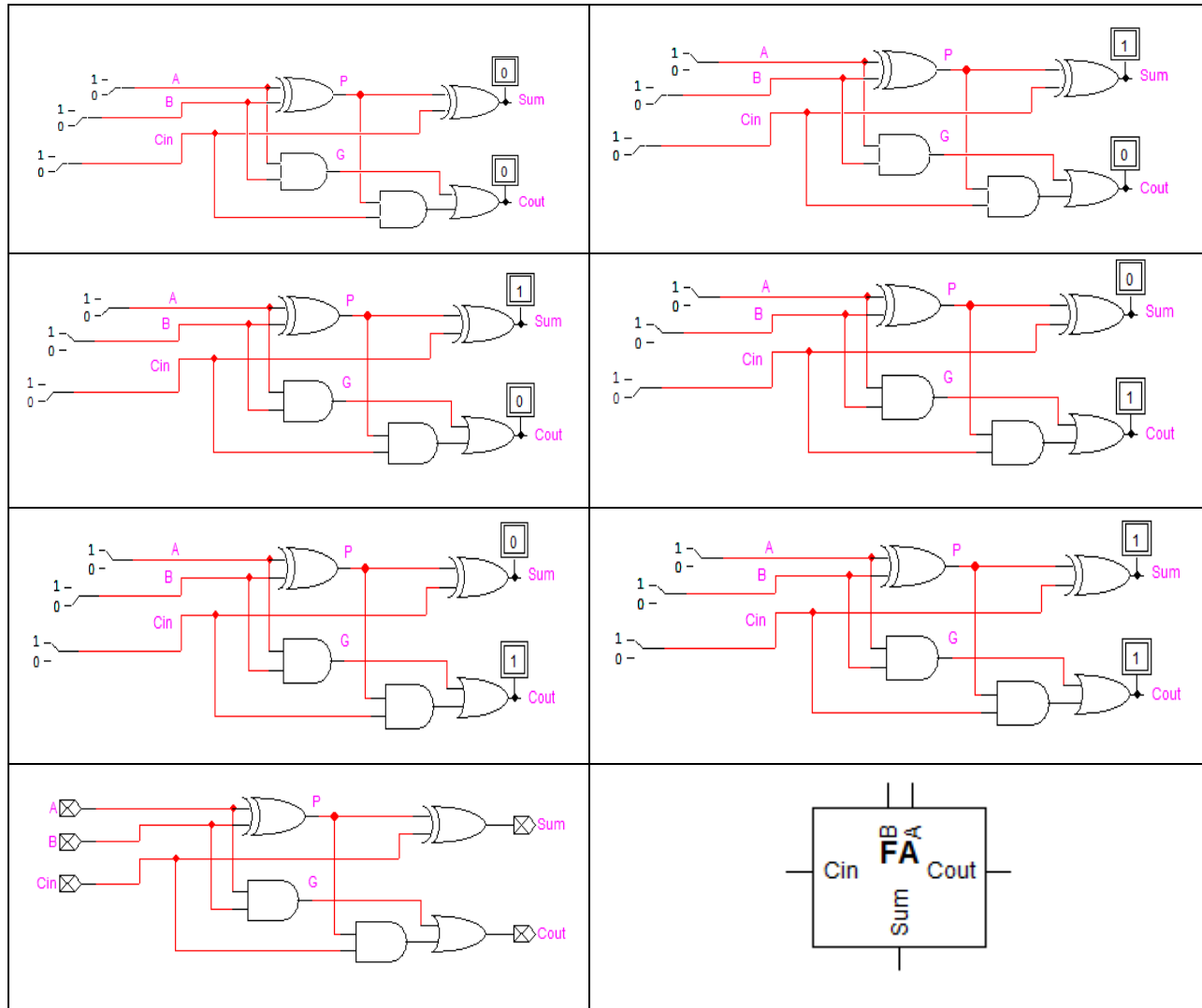
COE 202, Term 102
Fundamentals of Computer Engineering

Quiz# 4 (Take Home)

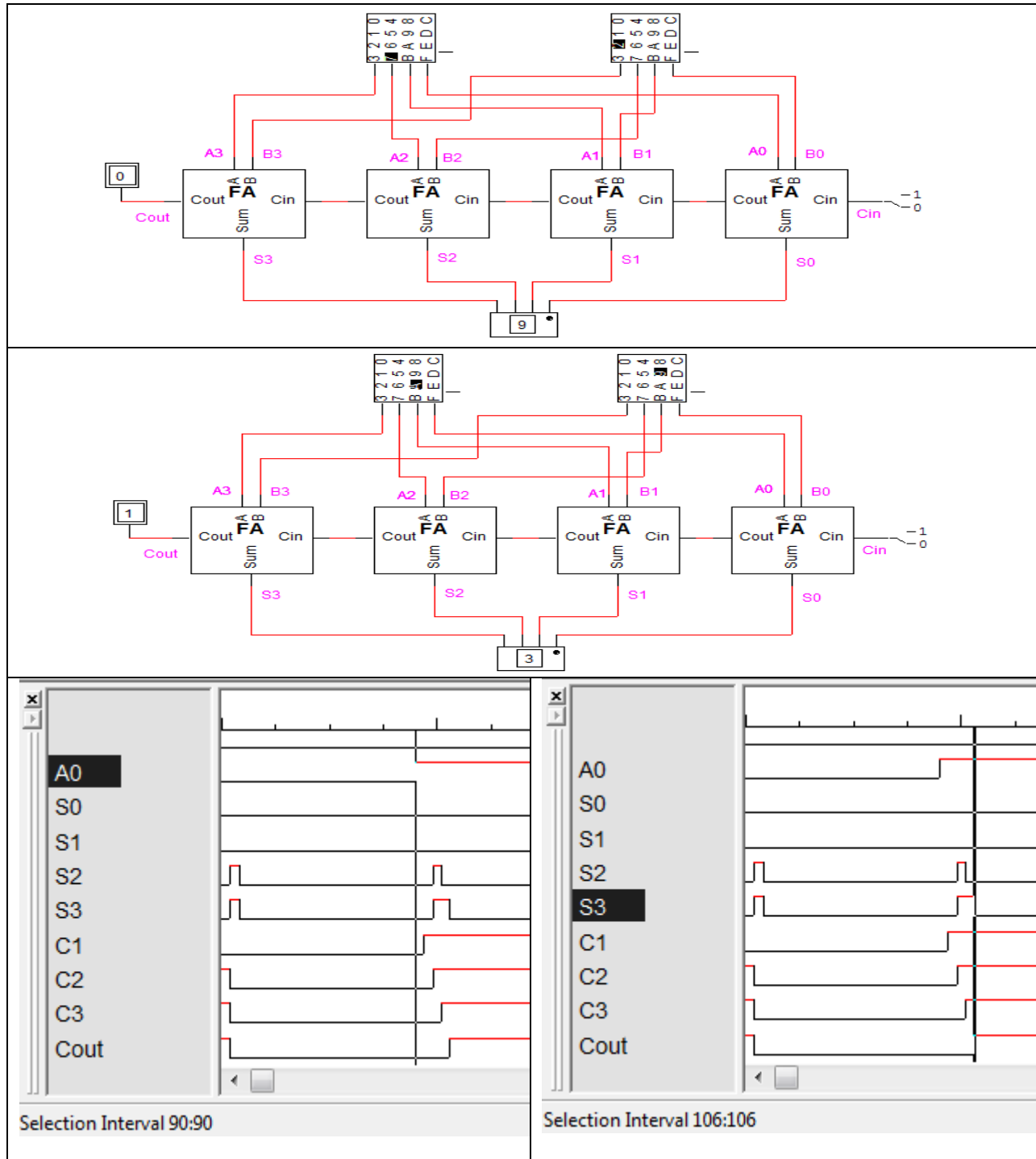
Due date: Monday, April 18, 2011

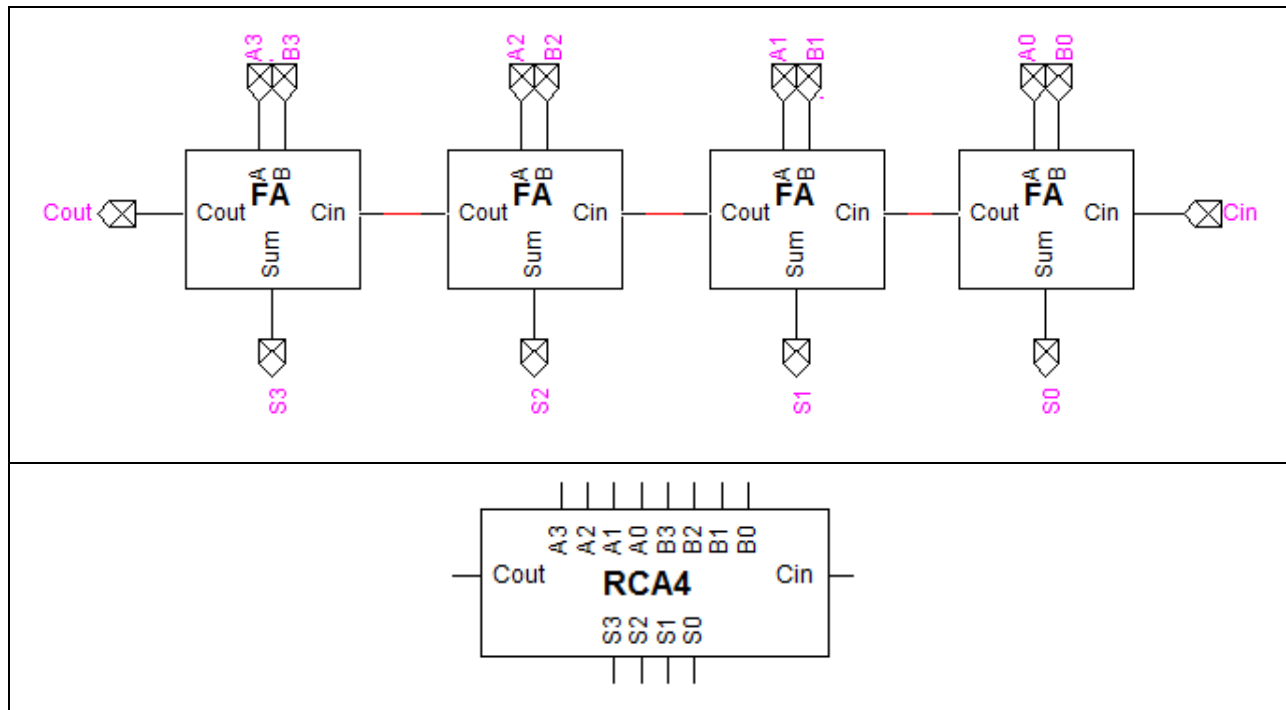
Q.1. Using logic works, you are required to do the following:

- a. Model a full adder circuit, verify its correct functionality by simulation. Add delay attributes to the gates by making the delay of a 2-input AND gate 2, the delay of a 2-input OR gate 2 and the delay of an XOR gate 4. Then create a device symbol for it.



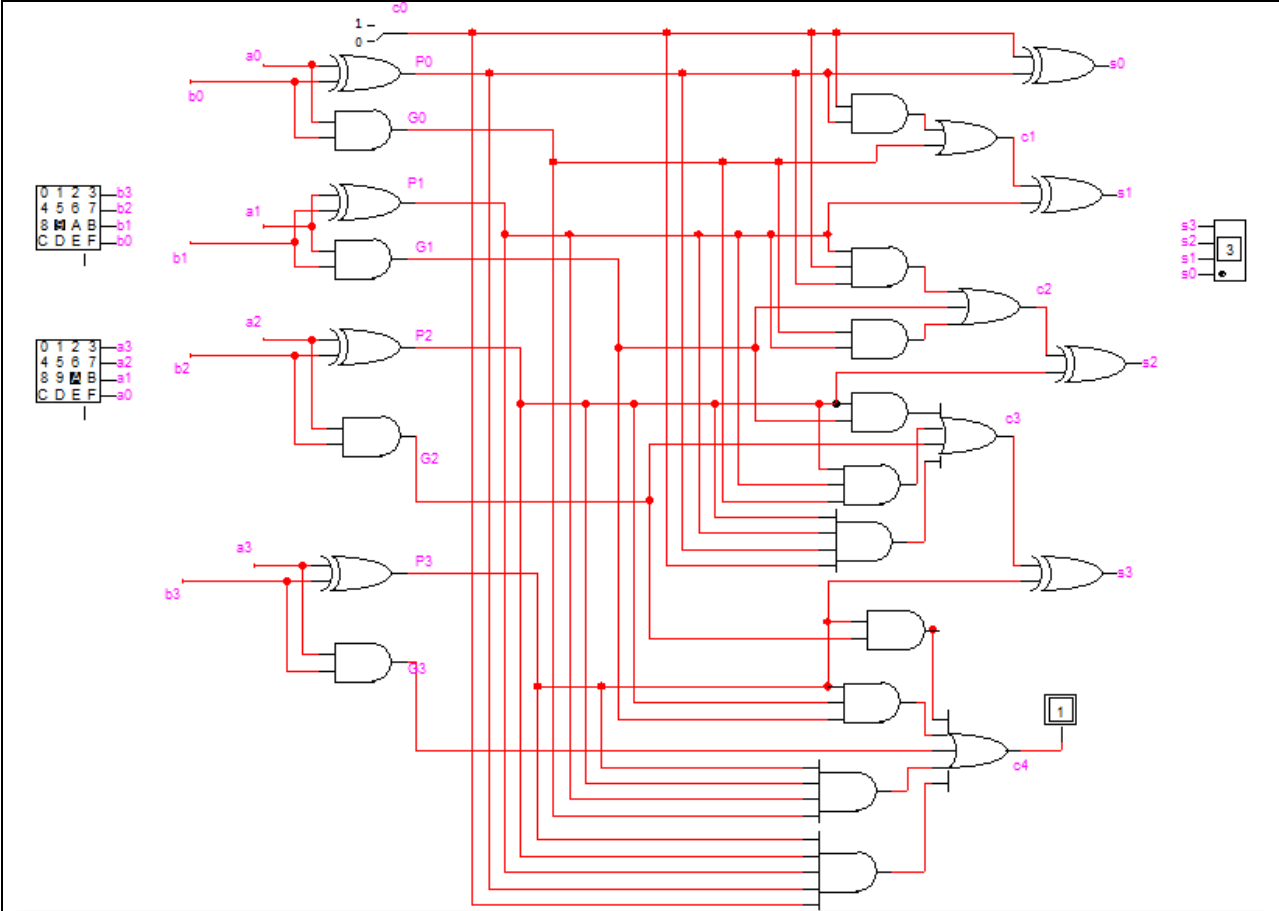
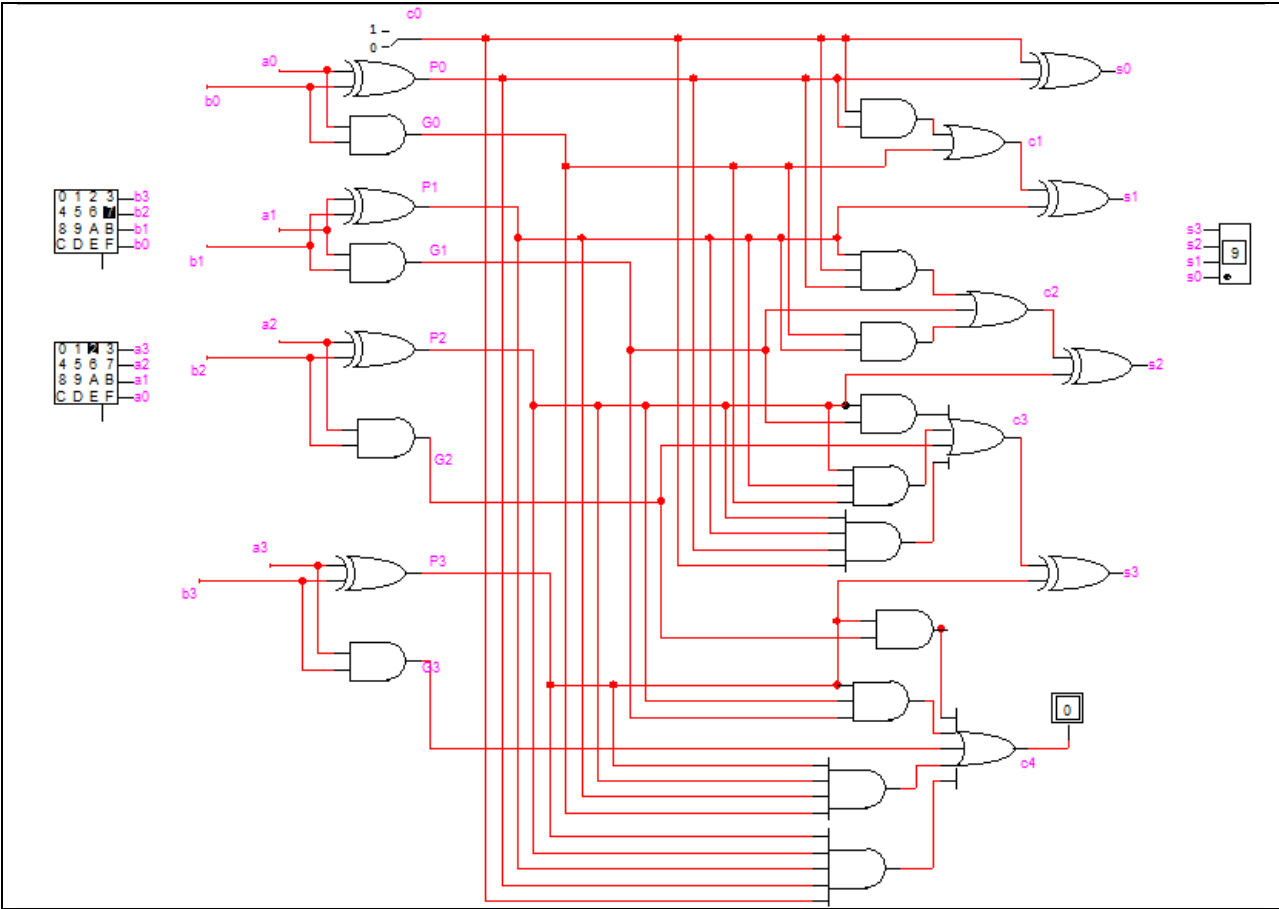
- b. Using the full adder created in (a) construct a 4-bit Ripple Carry Adder (RCA). Verify its correctness by simulation and determine the longest delay. Then, create a device symbol for it.

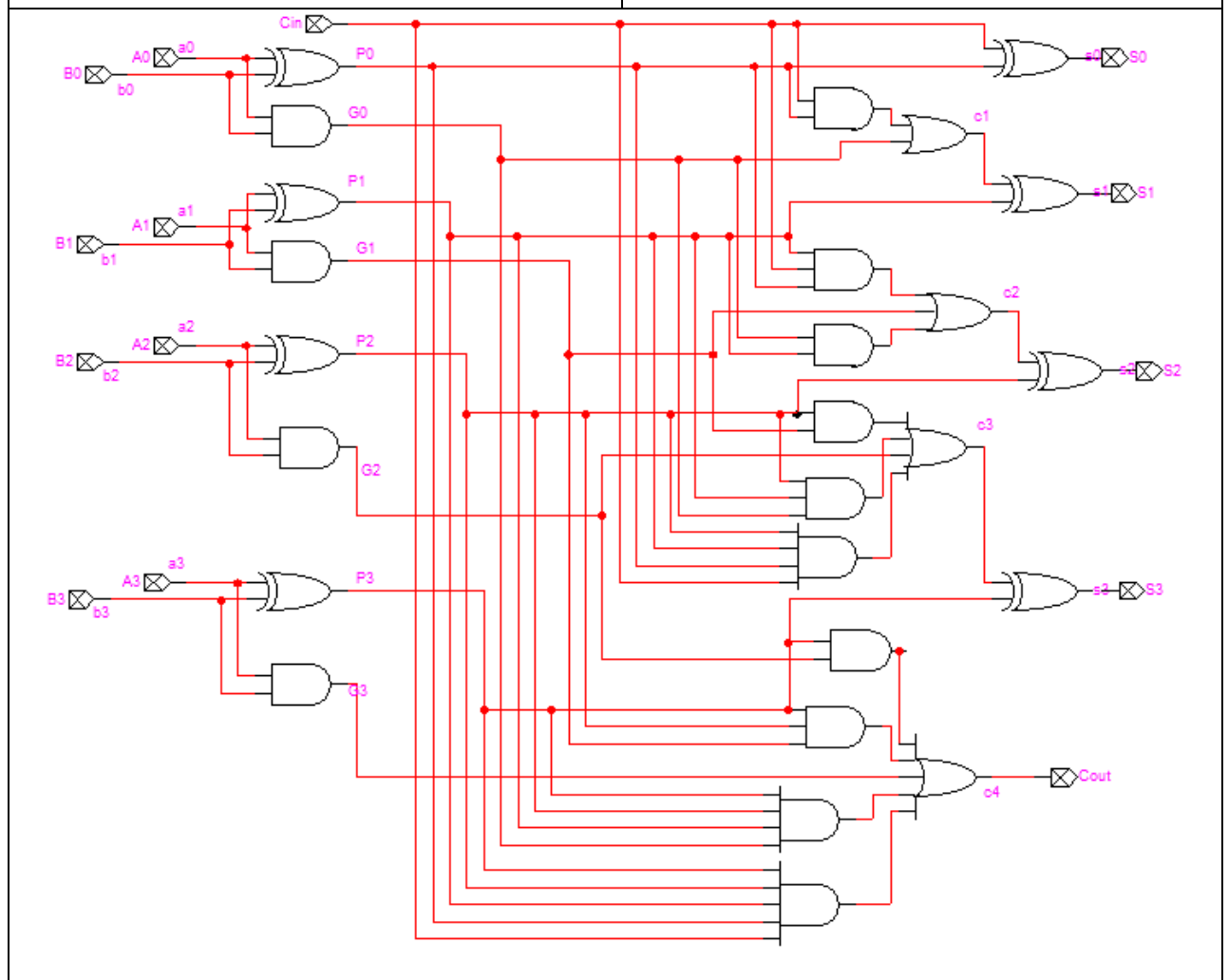
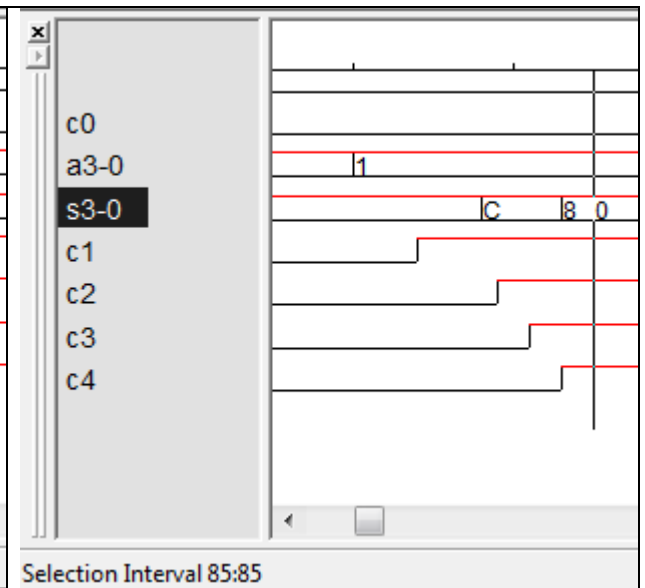
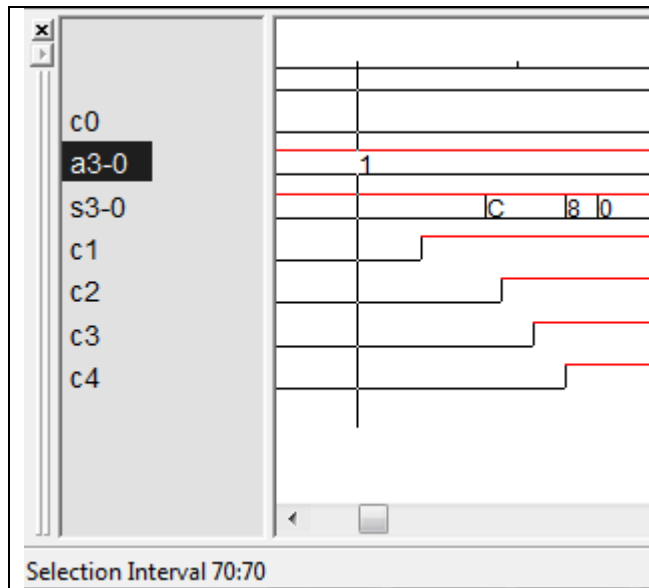


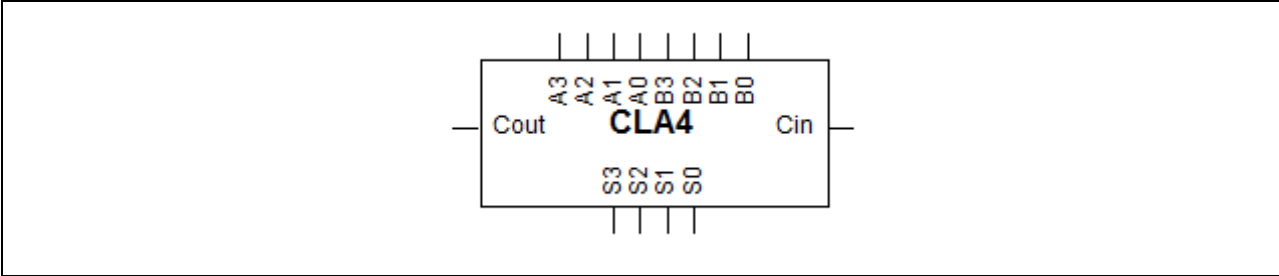


To measure the longest propagation delay, we set $B_3B_2B_1B_0=0000$ and $A_3A_2A_1A_0=0000$ and then change them to $B_3B_2B_1B_0=1111$ and $A_3A_2A_1A_0=0001$ to generate a carry in the first cell and propagate it to the last cell. To measure the longest delay we need to find the time difference between the time when A_0 has changed (time=90) to the time when $Cout$ or S_3 have changed (time=106)= $106-90=16$ ns. This is as expected as the generate AND gate in the first cell has a delay of 2ns and the carry is propagated after additional 2ns through the OR gate resulting in a total delay of 4ns from the first cell. Then, the AND and OR gates add a 4ns delay in each cell to propagate the carry which results in a delay of 16 ns.

- c. Model a 4-bit Carry Look-Ahead Adder (CLA) using the same gate delay attributes specified in (a). Verify its correctness by simulation and determine the longest delay. Compare its delay to the 4-bit RCA in (b). Then, create a device symbol for it.

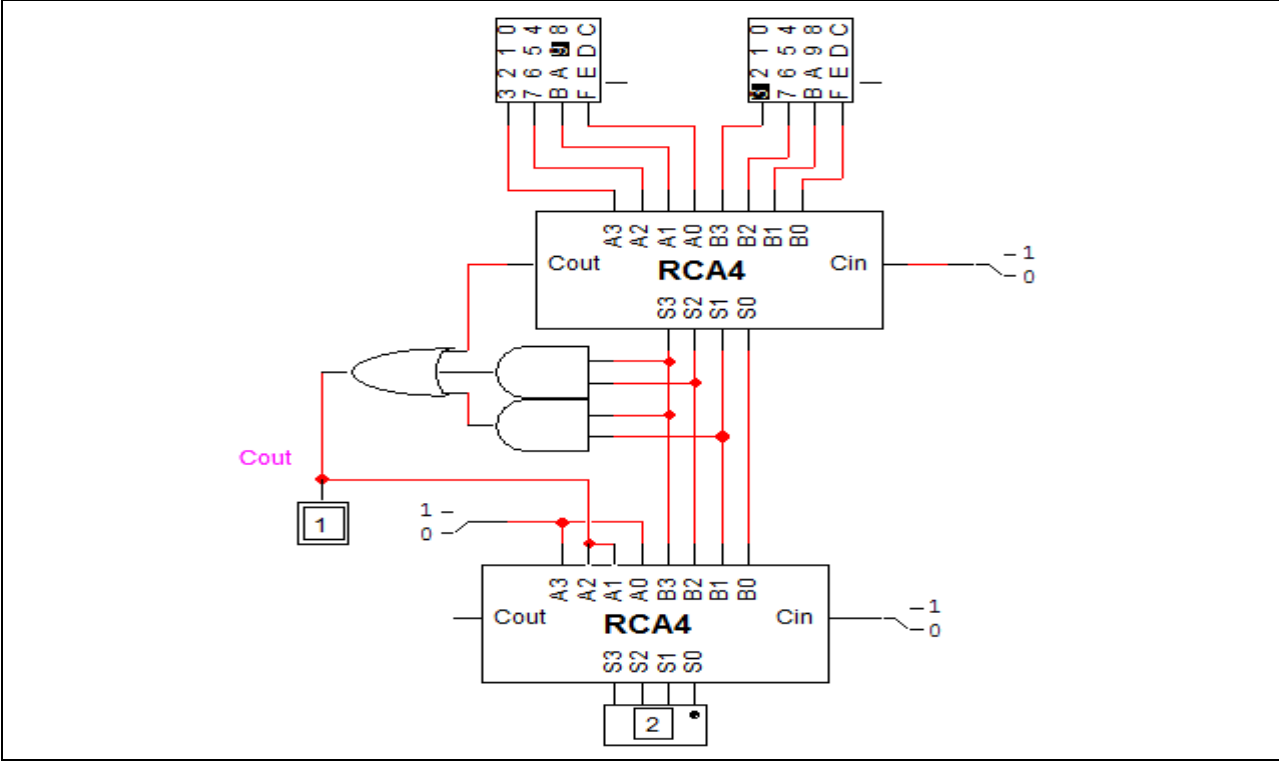


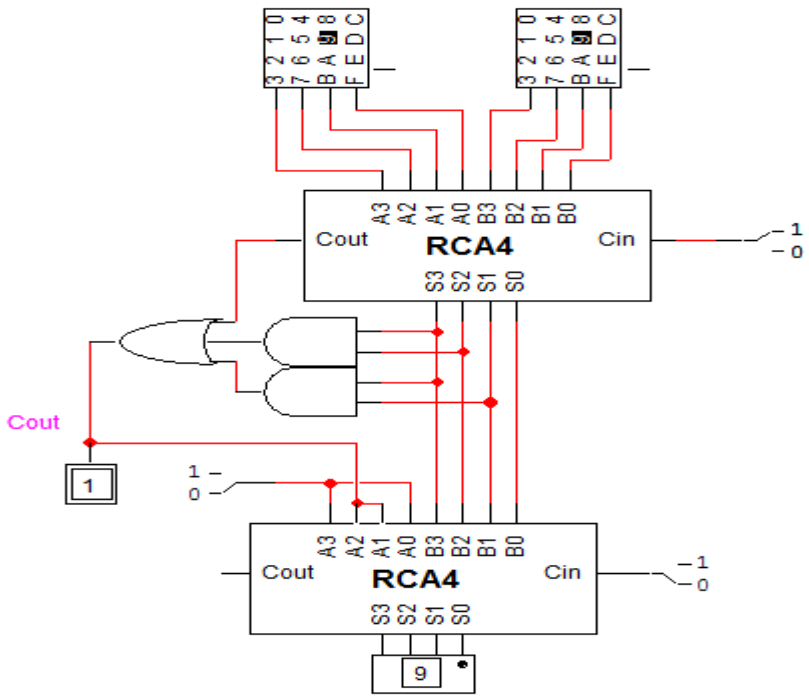
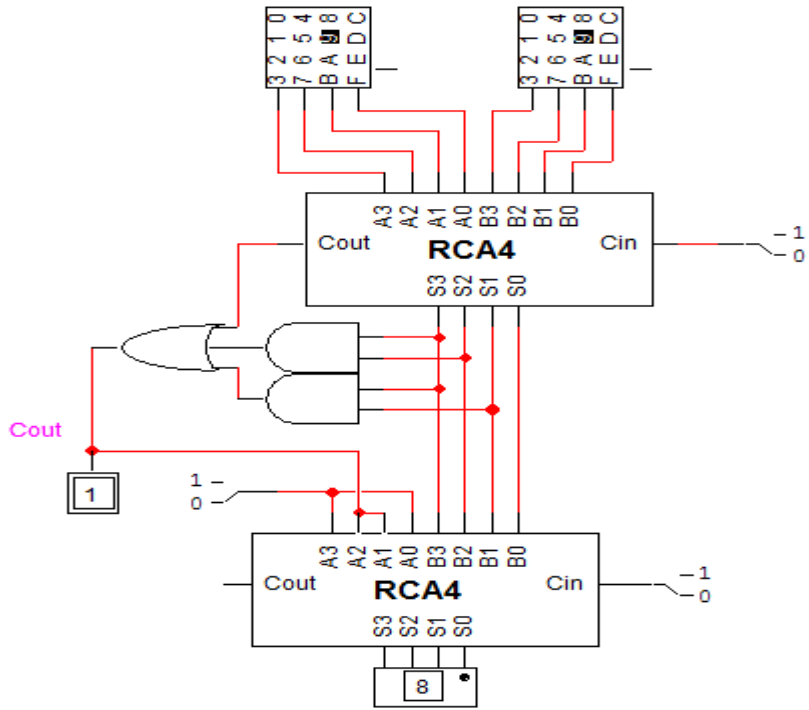




To measure the longest propagation delay, we set $B_3B_2B_1B_0=0000$ and $A_3A_2A_1A_0=0000$ and then change them to $B_3B_2B_1B_0=1111$ and $A_3A_2A_1A_0=0001$ to generate a carry in the first cell and propagate it to the last cell. To measure the longest delay we need to find the time difference between the time when A_0 has changed (time=70) to the time when S_3 has changed (time=85)= $85-70=15$ ns. We have the set delay of each AND & OR gate equal to the number of its inputs. Hence the delay for the carry signals is as follows: $C1=4$ ns; $C2=9$ ns; $C3=11$ ns; $C4=13$ ns. The delay for $S4=11+4=15$ ns. Note the delay compared the 4-bit RCA has improved only by 1 ns because we have set the delay of the XOR to 4ns. Usually the delay of the XOR is smaller and hence we get better delay improvements.

d. Model a BCD adder using the 4-bit RCA in (b) and verify its correctness by simulation.





e. Model a 4-bit by 4-bit multiplier using the 4-bit CLA adder in (c). Verify its correctness by simulation.

