Name: **Id#**

COE 200, Term 993
Fundamentals of Computer Engineering
Quiz# 4

Date: Sunday, July 30

Q.1. A reset-dominant flip-flop has set and reset inputs. It differs from a conventional SR flip-flop in that, when both S and R are equal to 1, the flip-flop is reset to 0.

(i) Obtain the characteristic table of the reset-dominant flip-flop.

(ii) Derive the excitation table for the reset-dominant flip-flop.

(iii) Design a positive-edge triggered reset-dominant flip-flop using JK-FF.

Q.2. A single-input, single-output sequential circuit is to be designed that recognizes only the input sequence 110011 applied to its inputs any time it occurs in the input stream. If the sequence is detected the output will be 1, otherwise it will be 0. Draw the state diagram for the sequence detector assuming overlapping of sequences i.e., the input sequence 1100110011 should produce the output sequence 0000010001.