Name: **Id#**

COE 202, Term 132
Digital Logic Design

Quiz# 4

Date: Tuesday, April 15

Q1. .Determine the decimal value of the 7-bit binary number (1011010) when interpreted as:

An unsigned number	A signed-magnitude number	A signed-1's complement number	A signed-2's complement number

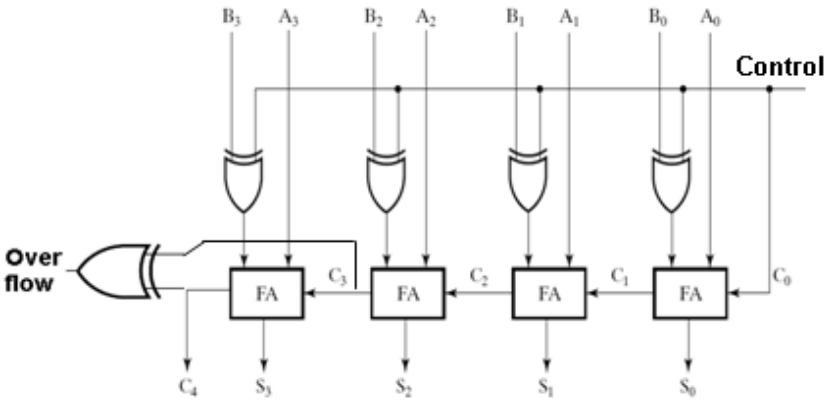
ii. Represent the decimal value (- 21) in binary using a total of 7 bits in the following notations:

A signed-magnitude number	A signed-1's complement number	A signed-2's complement number

iii. Perform the following signed-2's complement arithmetic operations in binary using 5 bits. All numbers given are represented in the signed-2's complement notation. Indicate clearly the carry values from the last two stages. For each of the three operations, check and indicate whether overflow occurred or not.

	a. 01101 +10110	b. 01010 - 11001	c. 11010 - 00100
Overflow Occurred? (Yes/No)			

(B) Consider the 2's complement 4-bit adder/subtractor hardware shown (**FA** = full adder).



i. Fill in the spaces in the table below.

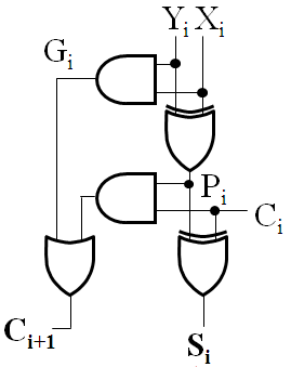
Inputs			Outputs			
A	**B**	Control	**S** (binary)	C_4	C_3	Overflow
0111	0101	0				
1010	1101	1				

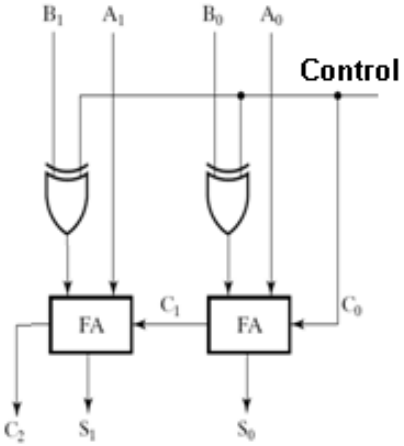
ii. What type of 4-bit adder is used in this design? (Circle the correct answer):

- Carry-ripple adder
- Carry-look-ahead adder

(C) Consider a 2-bit version of the hardware above which is shown below. Shown also is full adder used. Given that each basic gate (i.e. AND, OR, NOT) has a delay of τ ns and the XOR gate has a delay of 3τ:

The Full Adder (FA)





i. Express, as a function of τ, the longest time interval needed for the hardware to perform an operation on the two 2-bit numbers.

ii. If such an operation must be performed in no longer than 33 ns, calculate the maximum basic gate delay allowed.