Name: **Id#**

COE 202, Term 122
Digital Logic Design

Quiz# 4

Date: Monday, April 8

Q1. We would like to design an adder to add the 8-bit constant 10101010 to an arbitrary 8-bit number. The adder is to be designed using four identical adder modules, each of which will add 2 bits of the number to the constant (10) and a carry from the next lower pair of bits and produce 2 bits of the sum and the carry to the next bits. A block diagram of part of this design is shown below:
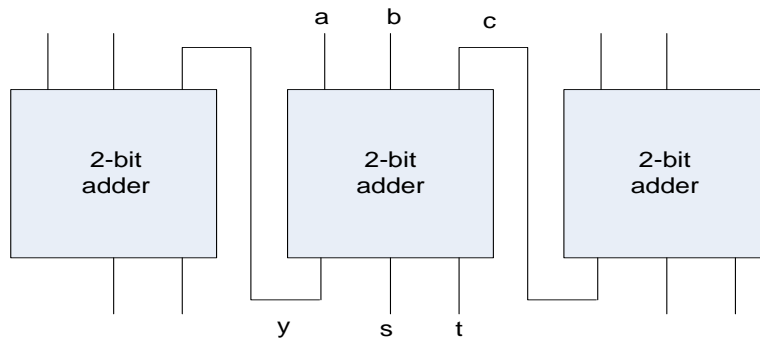
The problem each 2-bit adder solves is:

```
                        c
               a        b
   +           1        0
 ─────────────────────────────────────────────
        y      s        t
```

(i)   Show a truth table for the 2-bit adder (it has three inputs: a, b, and c, and it has three outputs: y, s, and t), and find minimal SOP expressions for each output.

(ii) Compute the delay from the c-input of each module to the y output of that module and the total delay for the 8 bits. Assume that the delay of a gate is related to the number of inputs i.e. the delay of an inverter is 1, the delay of a 2-input gate is 2, etc.

Q2.

(i) Determine the decimal value of the 7-bit binary number (1011010) when interpreted as:

An unsigned number	A signed-magnitude number	A signed-1's complement number	A signed-2's complement number

(ii) Represent the decimal value (- 21) in binary <u>using a total of 7 bits</u> in the following notations:

A signed-magnitude number	A signed-1's complement number	A signed-2's complement number

(iii) Perform the following signed-2's complement arithmetic operations in binary using 5 bits. All numbers given are represented in the signed-2's complement notation. Indicate clearly the <u>carry values from the last two stages</u>. For each of the three operations, check and indicate whether overflow occurred or not.

	a. 01101 +10110	b. 01010 - 11001	c. 11010 - 00100
Overflow Occurred? (Yes/No)			