

Name:

Id#

**COE 202, Term 112**  
**Digital Logic Design**

**Quiz# 4**

Date: Saturday, April 7

**Q1.**

i. Determine the decimal value of the 8-bit binary number (11010100) when interpreted as:

An unsigned number	A signed-magnitude number	A signed-1's complement number	A signed-2's complement number

ii. Represent the decimal value (- 40) in binary using a total of 8 bits in the following notations:

A signed-magnitude number	A signed-1's complement number	A signed-2's complement number

iii. Perform the following signed-2's complement arithmetic operations in binary using 5 bits. All numbers given are represented in the signed-2's complement notation. Indicate clearly the carry values from the last two stages. For each of the three operations, check and indicate whether overflow occurred or not.

	a. $\begin{array}{r} 01001 \\ +10111 \\ \hline \end{array}$	b. $\begin{array}{r} 01000 \\ -10010 \\ \hline \end{array}$	c. $\begin{array}{r} 11010 \\ -01101 \\ \hline \end{array}$
Overflow Occurred? (Yes/No)			

**Q2.** Design a combinational circuit that receives a 4-bit unsigned number  $\mathbf{I} = \mathbf{I}_3\mathbf{I}_2\mathbf{I}_1\mathbf{I}_0$  as input and generates the remainder of dividing this number by 3.