**Name: KEY** **Id#**

# COE 202, Term 121
# Digital Logic Design

## Quiz# 3

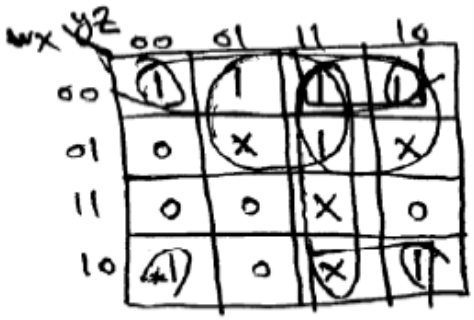
Date: Saturday, Nov. 10

**Q1**. For the Boolean function F(W, X, Y, Z)=Σ m(0, 1, 2, 3, 7, 8, 10), d(W, X, Y, Z)=Σ m(5, 6, 11, 15) shown in the k-map below:

| WX \ YZ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | 1 | 1 |
| 01 | 0 | x | 1 | x |
| 11 | 0 | 0 | x | 0 |
| 10 | 1 | 0 | x | 1 |

(i) Identify all the *prime implicants* and the *essential prime implicants* of F.

(ii) Simplify the Boolean function **F** into a minimal sum-of-products expression.

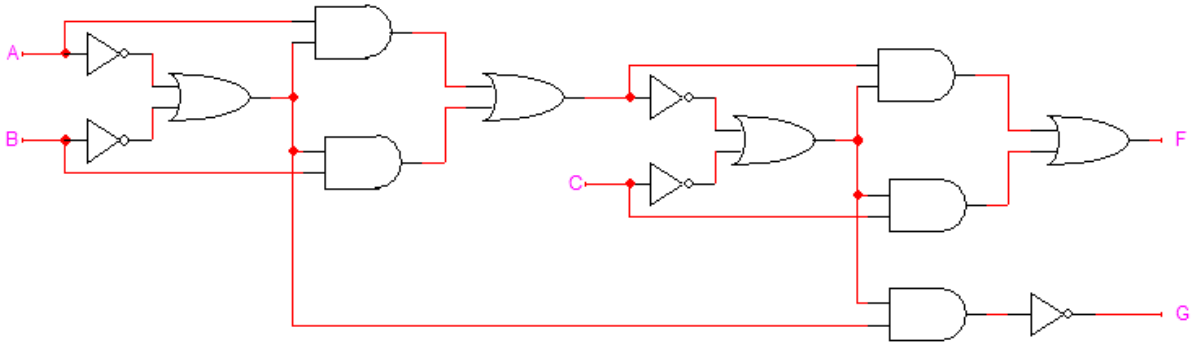


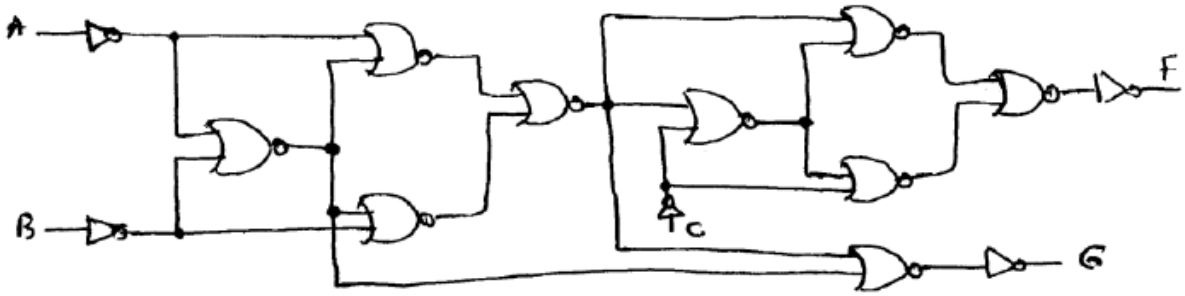

Prime implicants: $\bar{w}\bar{x}$, $\bar{x}\bar{z}$, $\bar{w}z$, $\bar{w}y$, $yz$, $\bar{x}y$

Essential prime implicants: $\bar{x}\bar{z}$

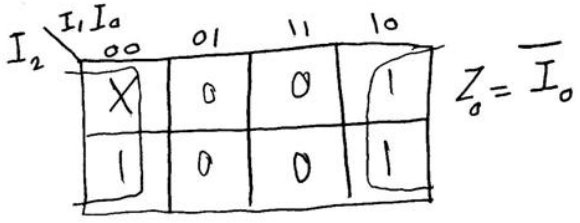
$F = \bar{x}\bar{z} + \bar{w}z$

**Q2**. Implement the logic circuit given below using only NOR and NOT gates

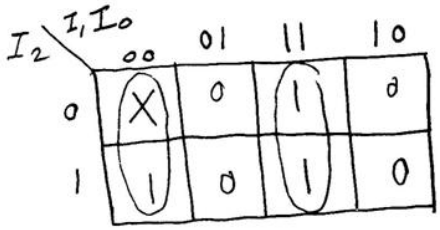


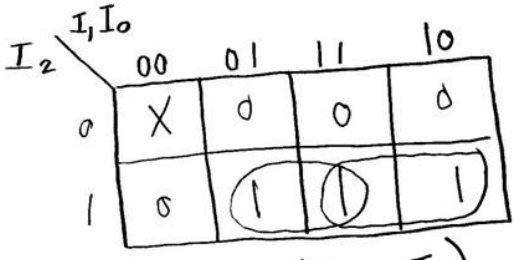
**Q3**. Design a 3-bit decrementer using only basic gates (AND, OR, and NOT). The circuit takes a 3-bit unsigned number $\mathbf{I=I_2I_1I_0}$ as input and generates a 3-bit output number $\mathbf{Z = Z_2Z_1Z_0}$ and a **Valid** output **V.** Whenever $\mathbf{I > 0}$ the output $\mathbf{Z = I-1}$ and $\mathbf{V=1}$. If $\mathbf{I=0}$, the output is invalid which is indicated by an output $\mathbf{V=0.}$ Derive the simplified Boolean expressions of all outputs.




$Z_0 = \overline{I_0}$




$Z_1 = \overline{I_1}\,\overline{I_0} + I_1\overline{I_0}$




$Z_2 = I_2 \cdot (I_0 + I_1)$

| $I_2$ | $I_1$ | $I_0$ | $Z_2$ | $Z_1$ | $Z_0$ | V |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | X | X | X | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | Ø | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | Ø | 1 |

$V = \text{Max\_Term } \emptyset$

$V = I_2 + I_1 + I_0$