Name: **Id#**
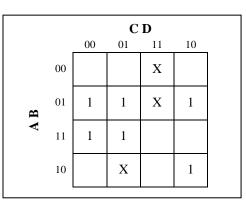
COE 202, Term 151
Digital Logic Design

Quiz# 3

Date: Sunday, Oct. 25

Q1. *Assuming the availability of all variables and their complements*, simplify the following two Boolean functions F and G subject to the given don't care conditions d1 and d2 using the K-Map method:

(a) Implement F using only <u>NOR</u> gates:

$F(A, B, C, D) = \Sigma(4, 5, 6, 10, 12, 13)$

$d1(A, B, C, D) = \Sigma(3, 7, 9)$

A B \ C D	00	01	11	10
00			X	
01	1	1	X	1
11	1	1		
10		X		1

(b) Implement G using only <u>NAND</u> gates:

$G(A, B, C, D) = \Sigma(0, 2, 8, 11, 13, 15)$

$d2(A, B, C, D) = \Sigma(3, 6, 7, 9, 12)$

A B \ C D	00	01	11	10
00	1		X	1
01			X	X
11	X	1	1	
10	1	X	1	

Q2. Implement the following circuit using only 2-input XOR gates with minimal number of gates: