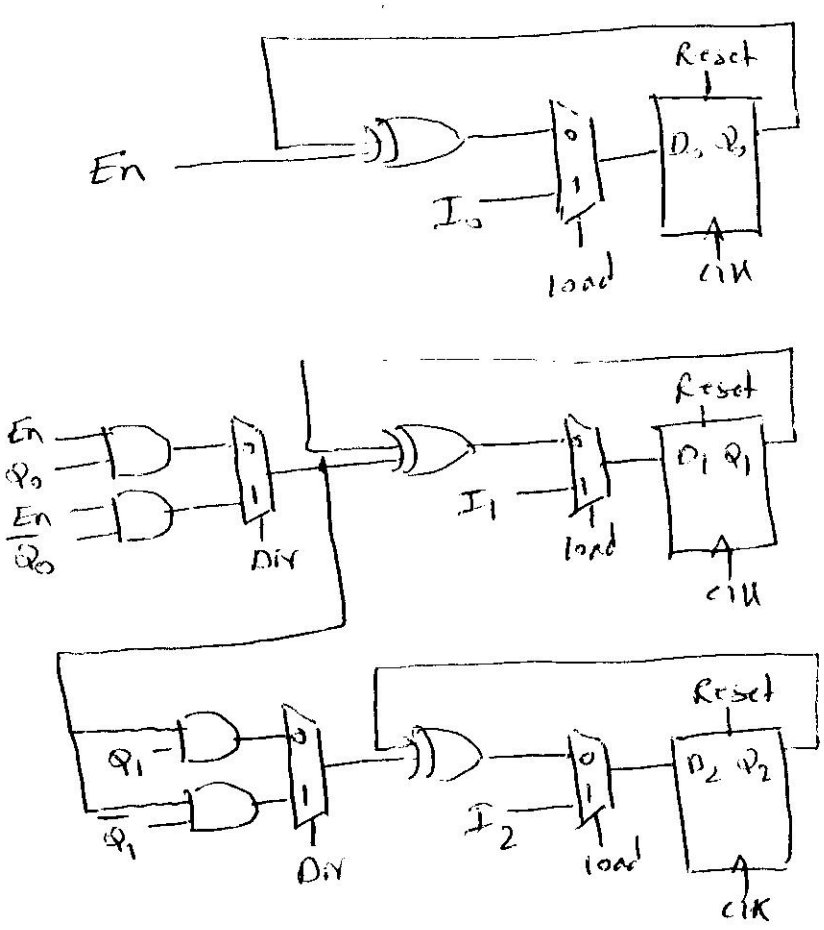
Name: KEY **Id#**

COE 202, Term 102
Fundamentals of Computer Engineering

Quiz# 10

Due date: Saturday, June 4, 2011

Q.1. Design a 3-bit synchronous counter with asynchronous reset signal, Reset, to reset it to the all 0 state, an enable signal, En, to control whether the counter maintains its state (En=0) or enabled to perform desired function (En=1), a parallel load signal, Load, to load it with any value, a Dir signal to control whether the counter counts up or down. When Dir=0 the counter counts up otherwise it counts down.



Q.2. Use the counter in (**Q.1**) to design a modular up/down counter that counts through the sequence {0, 1, 2, 3, 4, 5} up or down according to the signal Dir.