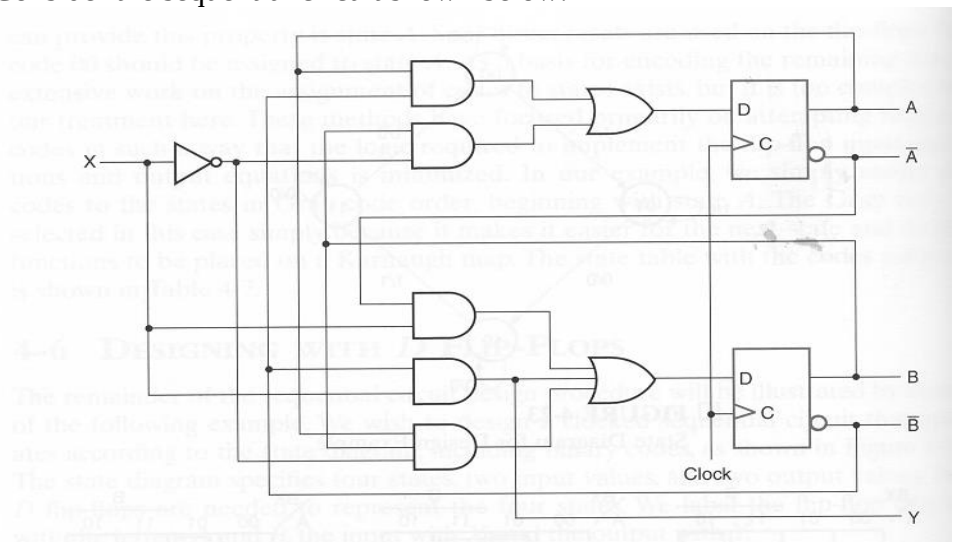
COE 202, Term 162

Digital Logic Design

HW# 7 Solution

Q.1. Consider the sequential circuit shown below:



(i) Starting from the state 00, determine the state transitions and output sequence that will be generated when the input sequence 11001101 is applied.

(ii) Determine the maximum clock frequency under which the circuit will operate correctly given that the propagation delay of the inverter gate is 2ns, the AND gate is 4ns, and the OR gate is 4ns. Assume that the D-FF has a setup time of 2ns, a hold time of 1ns, and a propagation delay of 2ns.

(i) $00 \xrightarrow[Y=1]{X=1} 01 \xrightarrow[Y=0]{X=1} 01 \xrightarrow[Y=0]{X=0} 10 \xrightarrow[Y=0]{X=0} 10$

$10 \xrightarrow[Y=1]{X=1} 11 \xrightarrow[Y=0]{X=1} 00 \xrightarrow[Y=0]{X=0} 00 \xrightarrow[Y=1]{X=1} 01$

(ii) For the circuit to operate correctly, the clock period T has to satisfy the following constraint:

$$T > t_{ff}^{max} + t_c^{max} + t_{su}^{max}$$

$t_{ff}^{max} = 2\,ns$

$t_c^{max} = \max(t_{c1}, t_{c2})$

$t_{c1} = 4\,ns$

$t_{c2} = 2ns + 4ns + 4ns = 10\,ns$

$t_c^{max} = 10\,ns$

$t_{su}^{max} = 2\,ns$

Thus, $T > 2ns + 10ns + 2ns = 14ns$

The maximum frequency $f = \frac{1}{T} < \frac{1}{14ns} = 71.4\,MHz$

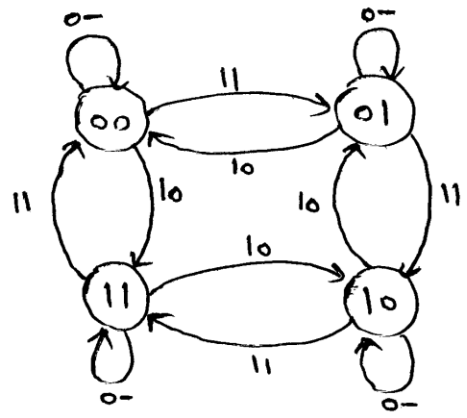
If we add a 10% safety margin, then $T = 15.4ns$

and $f = 65\,MHz$

Note $t_h^{min} = 2ns < t_{ff}^{min} + t_c^{min} = 2ns + 8ns = 10ns$

So, the hold time constraint is satisfied.

Q.2. Design a sequential circuit with two flip-flops A and B and two inputs E and X. If E=0, the circuit remains in the same state, regardless of the value of X. When E=1 and X=1, the circuit goes through the state transitions from 00 to 01 to 10 to 11, back to 00, and then repeats. When E=1 and X=0, the circuit goes through the state transitions from 00 to 11 to 10 to 01, back to 00, and then repeats. Design the circuit using Positive-edge-triggered D-FF.

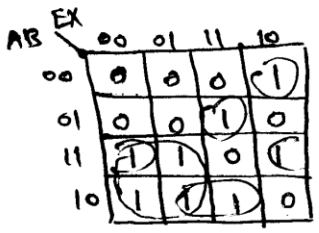


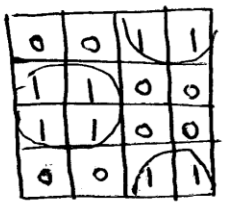
State Diagram

- State table:

current State		next State			
A	B	EX=00	EX=01	EX=10	EX=11
0	0	0 0	0 0	1 1	0 1
0	1	0 1	0 1	0 0	1 0
1	0	1 0	1 0	0 1	1 1
1	1	1 1	1 1	1 0	0 0

Design with positive-edge-triggered D-FF





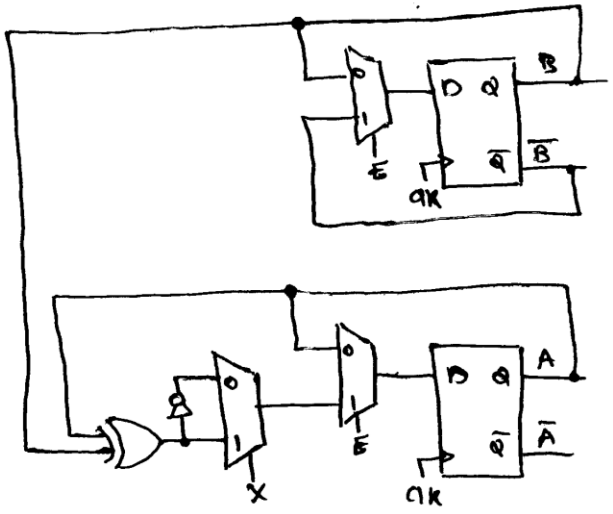
$$D_A = A\bar{E} + A\bar{B}X + AB\bar{X} + \bar{A}BEX + \bar{A}\bar{B}E\bar{X}$$

$$D_B = B\bar{E} + \bar{B}E$$

OR

$$D_A = A\bar{E} + XEA\bar{B} + AB\bar{X}E + \bar{A}BEX + \bar{A}\bar{B}E\bar{X}$$

$$= A\bar{E} + E[\bar{X}[AB + \bar{A}\bar{B}] + X[A\bar{B} + \bar{A}B]]$$

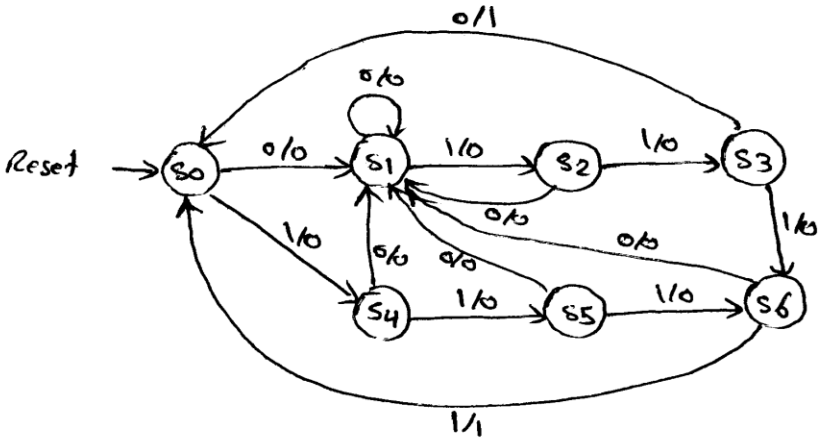


Q.3. A single-input, single-output sequential circuit is to be designed that recognizes only the two input sequences 0110 and 1111 applied to its inputs any time they occur in the input stream. If any of these two sequences is detected the output will be 1, otherwise it will be 0.

(i) Show the state diagram for this circuit assuming no detection of overlapping sequences.

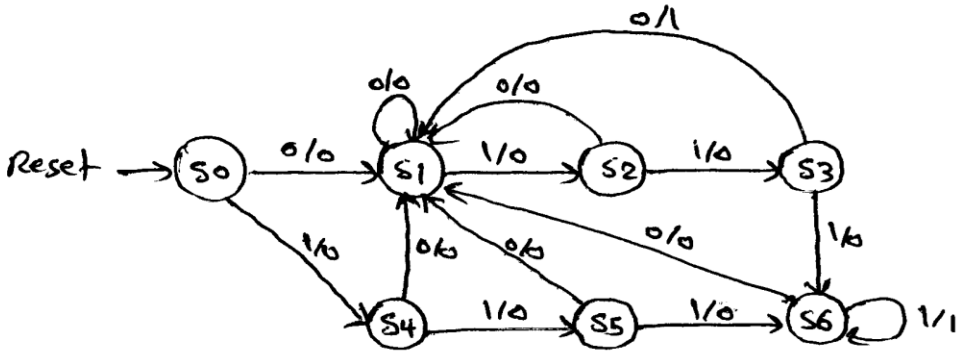
(ii) Show the state diagram for this circuit assuming detection of overlapping sequences.

(i) State diagram with no overlapping:



Note that it is assumed here that state S0 is the reset state, i.e. when the Reset input is high the machine will start from state S0.

(ii) State diagram with overlapping:

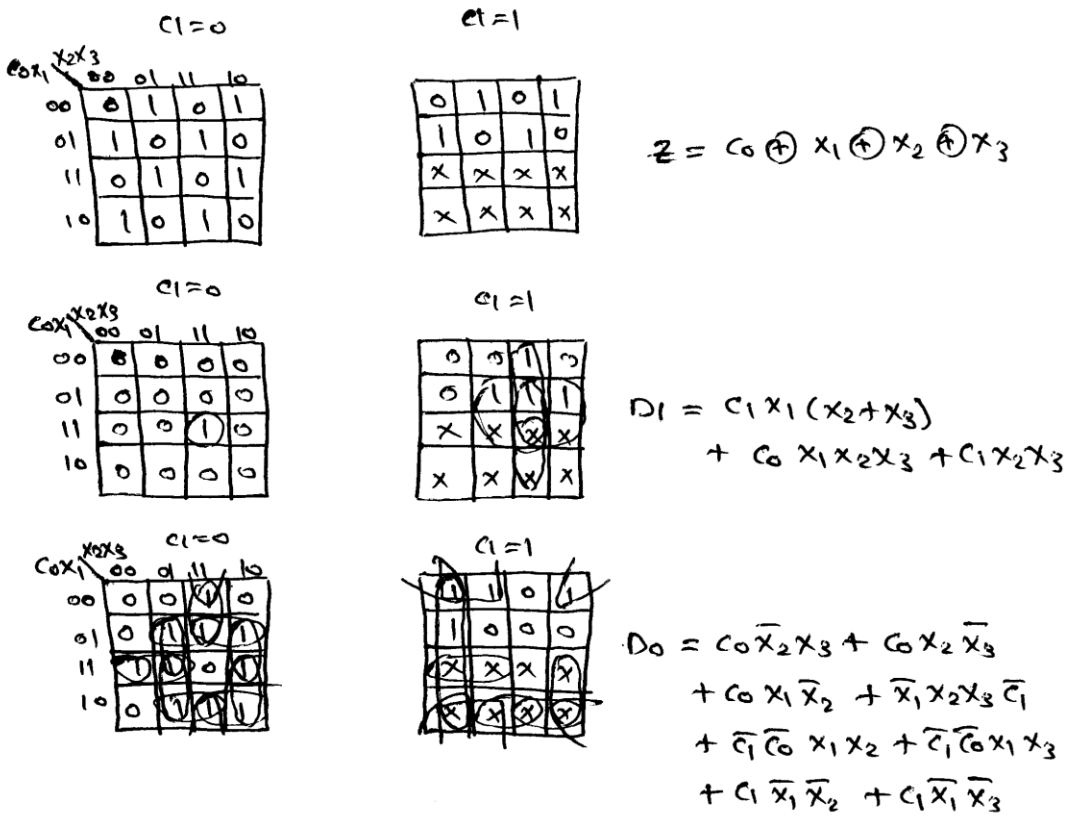


Q.4. You are to design a serial adder A3 that computes the sum of three separate serial input streams rather than the usual two. The adder has three primary inputs X_1, X_2, X_3, and a single primary output Z. Using D flip-flops and any standard gates, construct the state table, transition table, and a logic circuit diagram for A3.

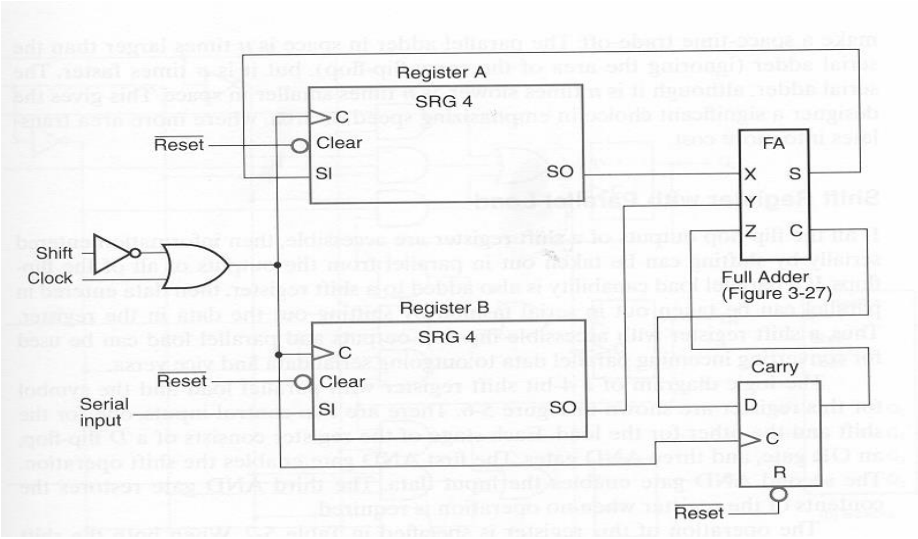
Note that in the design of a 3-input serial adder, it is not sufficient to use a single bit for holding the carry out of addition. It is necessary to use two bits to represent the carry out as its value is greater than 1.

State table:

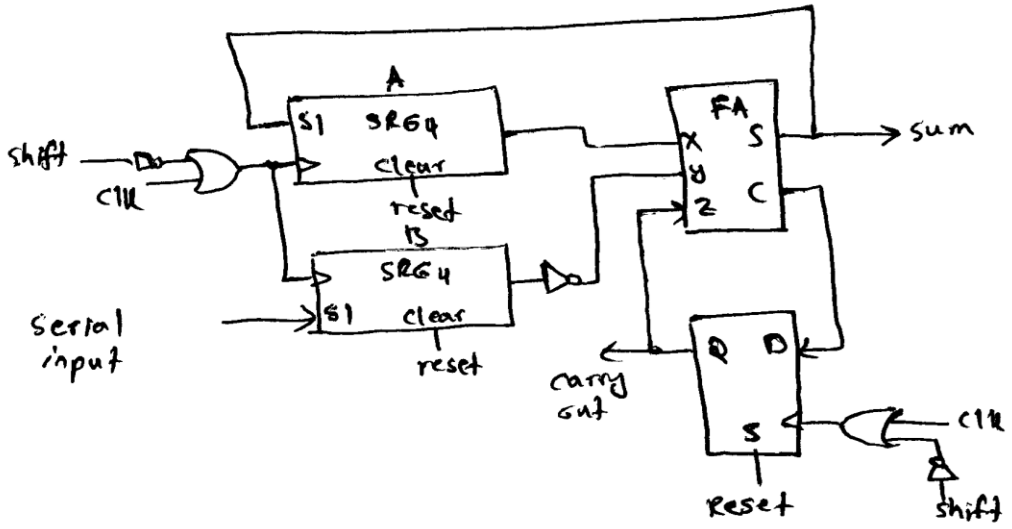
Current state		Input			Next state		Output
C_1	C_0	X_1	X_2	X_3	C_1	C_0	Z
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	0	0	1	0
0	0	1	1	1	0	1	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	0	1	1
0	1	1	0	0	0	1	0
0	1	1	0	1	0	1	1
0	1	1	1	0	0	1	1
0	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	0	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	0	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	1



Q.5. What changes are needed in the figure shown below to convert it to a serial subtractor that subtracts the contents of register B from the contents of register A. Explain how it is possible to detect whether A < B. If A < B, what will be the relationship of the result of the subtraction to the correct result?



The serial adder can be converted to a serial subtractor as follows:

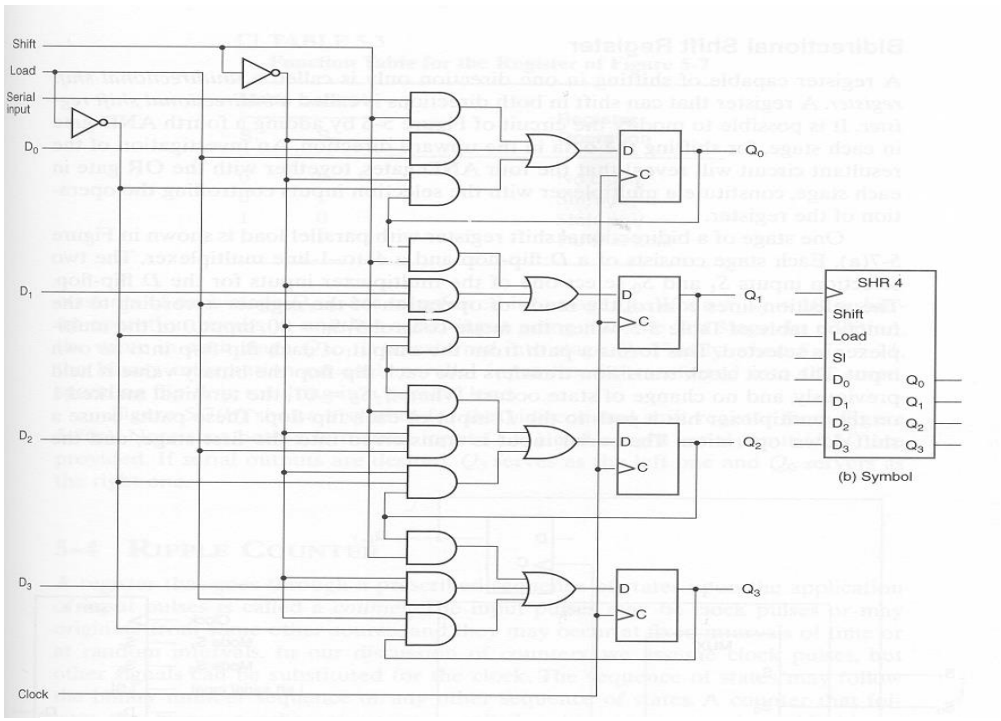


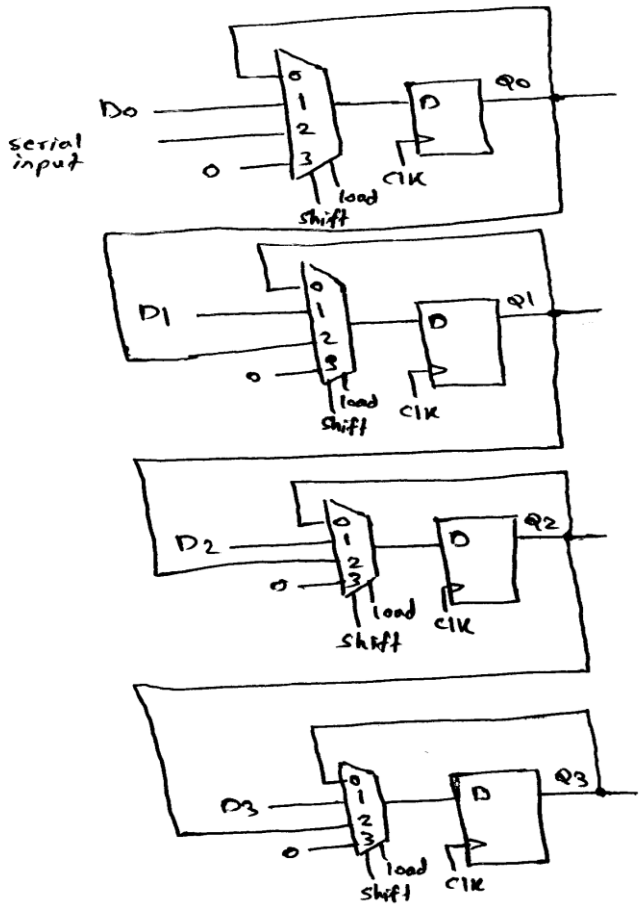
Note that when Reset is set to high, the FF will be set to high i.e. the carry value will be 1.

Thus, $A + \overline{B} + 1 = A - B$.

Q.6. Modify the register shown below so that it will operate according to the following function table using selection inputs s_1 and s_0.

S_1	S_0	Register Operation
0	0	No change
0	1	Clear register to 0
1	0	Shift down
1	1	Load parallel data


Shift
Load
Serial input
D_0
D_1
D_2
D_3
Clock
D
C
Q_0
Q_1
Q_2
Q_3
SHR 4
Shift
Load
SI
D_0
D_1
D_2
D_3
Q_0
Q_1
Q_2
Q_3
(b) Symbol


serial input
D0
D1
D2
D3
0
1
2
3
load
Shift
CLK
D
Q0
Q1
Q2
Q3