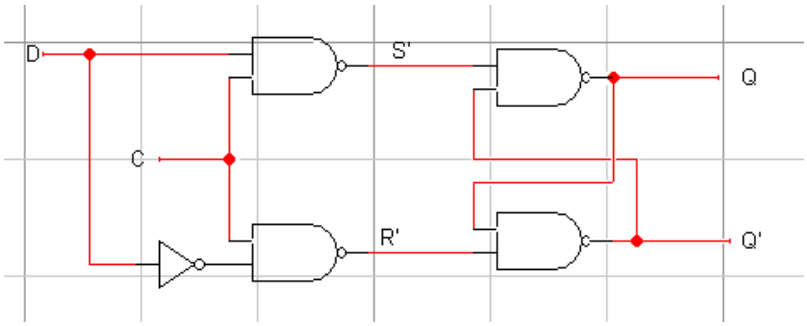
COE 202, Term 162

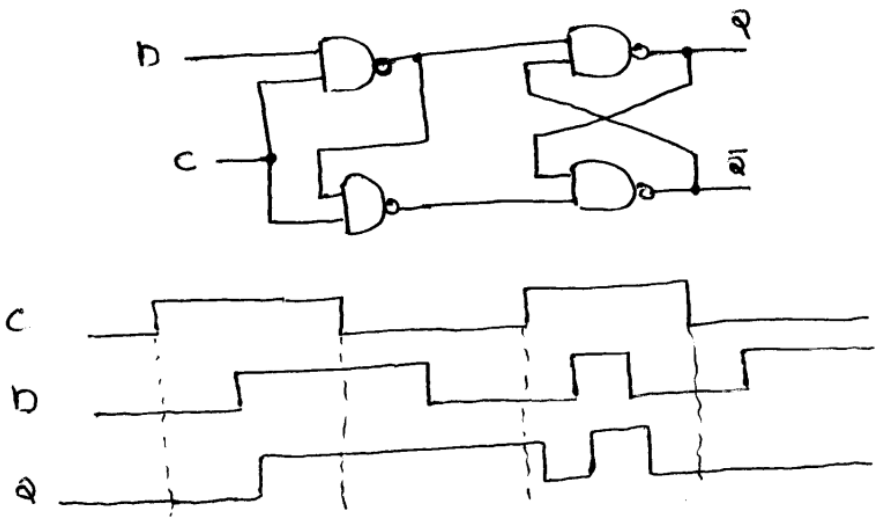
Digital Logic Design

HW# 6 Solution

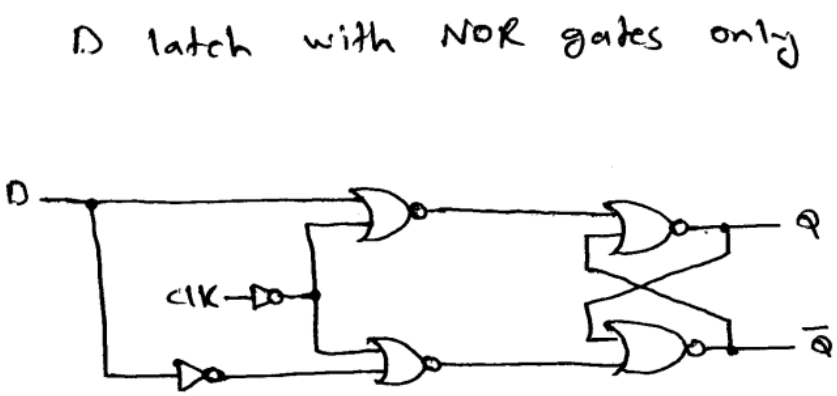
Q.1. The D-latch shown below can be constructed with only four NAND gates. This can be done by removing the inverter and connecting the output of the upper NAND gate (connected to the D input) to the input of the lower NAND gate (Connected to D'). Use manual or computer-based logic simulation to verify that the new circuit is functionally the same as the original one.



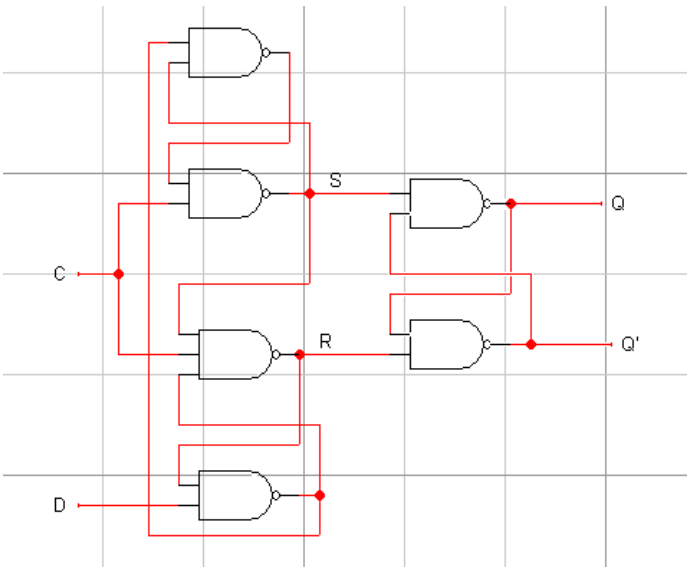
Modified D-latch

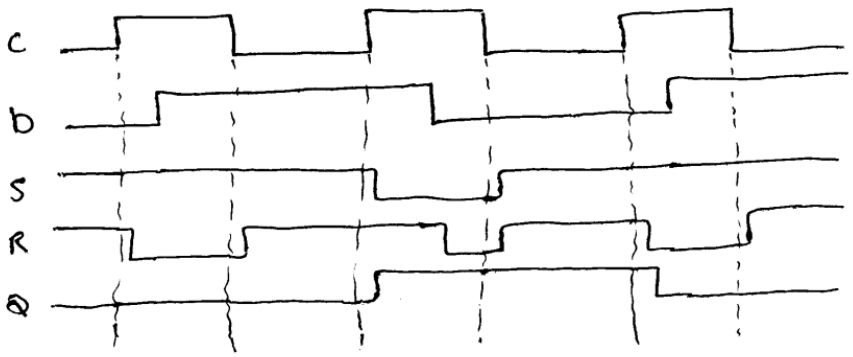


Q.2. Obtain the logic diagram of the D-latch give in Q1, using NOR gates only.



Q.3. A popular alternative design for positive-edge-triggered D flip-flop is shown below. Simulate the circuit to determine that its functional behavior is identical to that of a D flip-flop.





Q.4. A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:

$D_A = X` Y + X A$ $D_B = X` B + X A$ $Z = B$

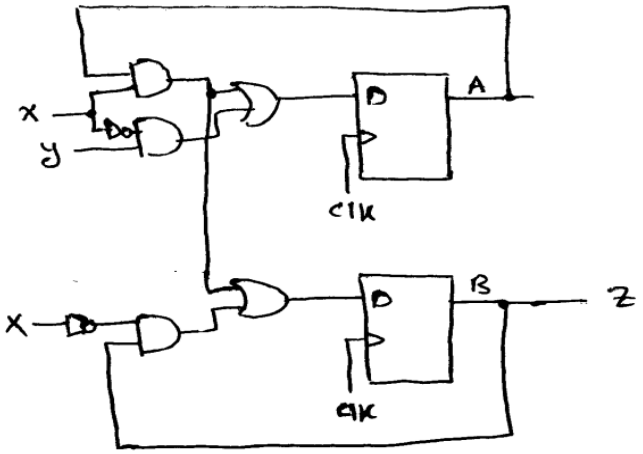
(i) Draw the logic diagram of the circuit.

(ii) Derive the state table.

(iii) Derive the state diagram.

$D_A = \bar{x}y + xA$, $D_B = \bar{x}B + xA$, $z = B$

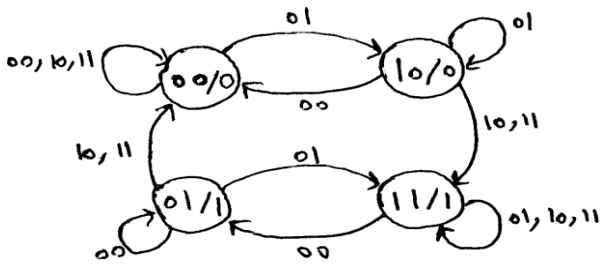
(a)



(b) State Table:

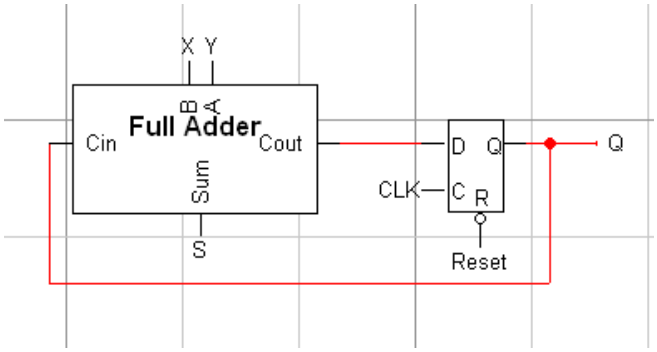
Current State AB	Next State xy=00 AB	Next State xy=01 AB	Next State xy=10 AB	Next State xy=11 AB	output z
0 0	0 0	1 0	0 0	0 0	0
0 1	0 1	1 1	0 0	0 0	1
1 0	0 0	1 0	1 1	1 1	0
1 1	0 1	1 1	1 1	1 1	1

(c) State Diagram:



* Note that this circuit has a Moore model.
* Note that this circuit has several synchronizing sequences. For example, {00, 11} synchronizes it to state 00.

Q.5. A sequential circuit has one flip-flip Q, two inputs X and Y, and one output S. The circuit consists of a full adder circuit connected to a D flip-flop, as shown below. Derive the state table and state diagram of the sequential circuit.



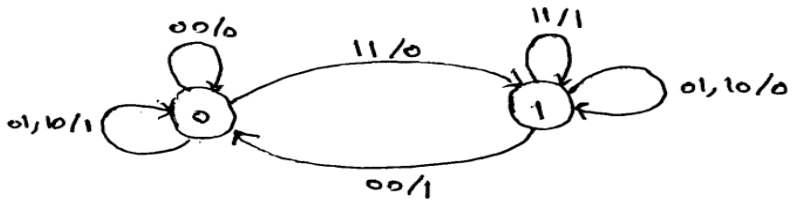
$$D_z = xy + xz + yz$$

$$S = x \oplus y \oplus z$$

State Table:

Current state	Inputs		Next state	output
z	x	y	z	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

State Diagram:



This circuit is a mealy model.

Note that this circuit has synchronizing sequence. For example, {00} synchronizes the circuit to state 0. Also, {11} synchronizes it to the 1 state.