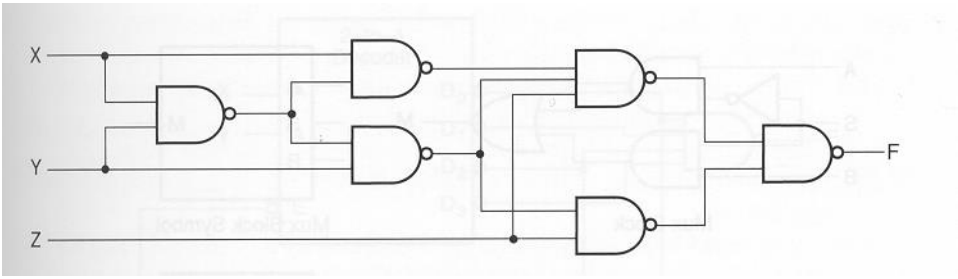
COE 202, Term 162

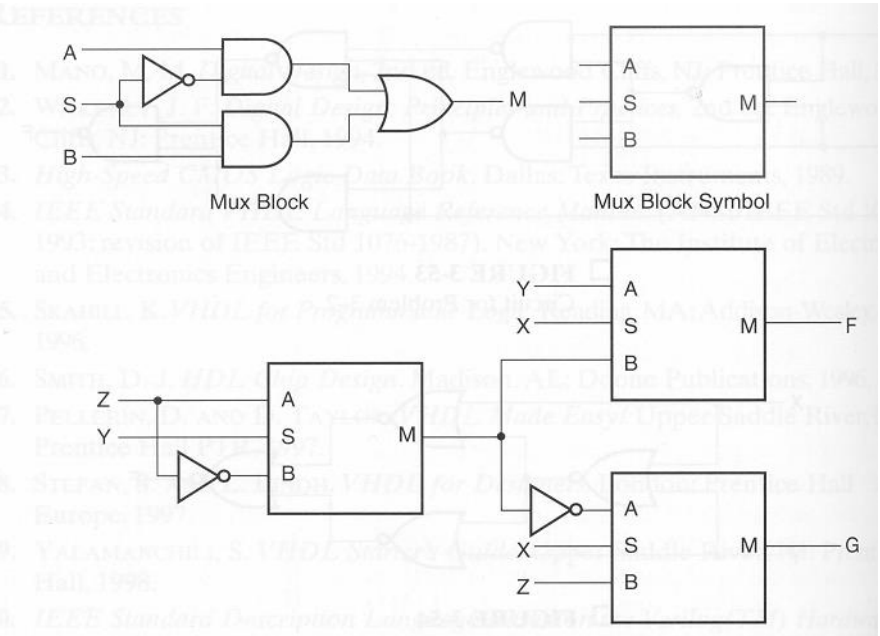
Digital Logic Design

HW# 5 Solution

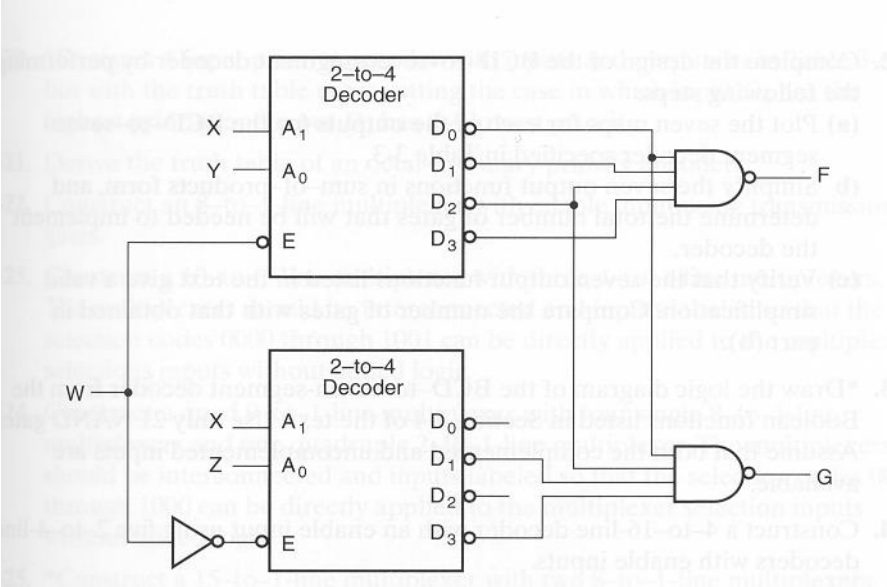
Q.1. Obtain the truth table for the circuit shown below. Draw an equivalent circuit for F with fewer NAND gates.



Q.2. Find simplified Boolean equations for the outputs F and G of the hierarchical circuit given below.



Q.3. Find the truth table for the outputs F and G of the hierarchical circuit shown below.



Q.4. Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable input and one 2-to-4 line decoder.

Q.5. A Combinational circuit is defined by the following three Boolean functions:

$F_1(X, Y, Z) = X`Y` + XYZ`$
$F_2(X, Y, Z) = X` + Z$
$F_3(X, Y, Z) = XY + X`Y`$

(i) Design the circuit with a 3x8 decoder, four 2-input OR gates, and an inverter.

(ii) Design the circuit with two 4x1 MUXs, one 2-input OR gate, and an inverter.

Q.6. Design a 4-input priority encoder with four inputs and three outputs including the valid bit but with the truth table representing the case in which input D_0 has the highest priority and input D_3 has the lowest priority.

Q.7. Construct a quad 9-to-1 line multiplexer with four single 8-to-1 line multiplexers and one quadruple 2-to-1 line multiplexer. The multiplexers should be interconnected and inputs labeled so that the selection codes 0000 through 1000 can be directly applied to the multiplexer selection inputs without added logic.

Q.8. Implement the following Boolean function $F(A, B, C, D)=\Sigma\, m(4, 6, 7, 8, 12, 15)$ with:

(i) An 8x1 MUX. Assume that the inputs A, B, and C are used for the select lines.

(ii) A 4x1 MUX and external gates. Assume that the inputs A and B are used for the select lines.

Q.9. Design a Combinational circuit that accepts a 3-bit number and generates as output a binary number equal to the square of the input number.

Q.10. It is required to design a Combinational circuit that compares two n-bit numbers to see if they are equal or not. Design a circuit that has three inputs and one output, that can be used for each of the n bits, such that the circuit is connected in cascade by carry-like signals. One of the inputs to each cell is a carry input, and the single output is a carry output.

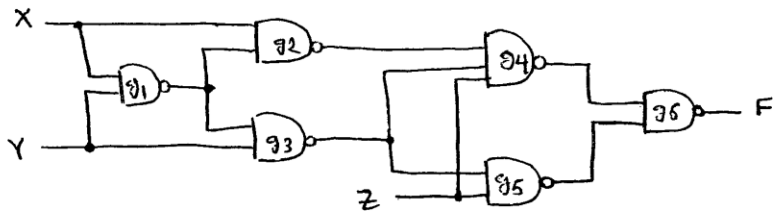
Q.11. Design three versions of the combinational circuit whose input is a 4-bit number and whose output is the 2's complement of the input number such that:

(i) The circuit is a simplified two-level circuit, plus inverters as needed for the input variables.

(ii) The circuit is made up of four identical two-input, two output cells, one for each bit. The cells are connected in cascade, with lines similar to a carry between them. The value applied to the rightmost carry bit is 0.

(iii) The circuit is redesigned with carry lookahead-like logic in order to speed up the circuit in part (ii) for use in larger circuits with 4n input bits.

Q1



$g_1 = (X \cdot Y)'$

$g_2 = XY + \bar{X} = Y + \bar{X}$

$g_3 = XY + \bar{Y} = X + \bar{Y}$

$g_4 = (g_2 \cdot g_3 \cdot Z)' = [(Y+\bar{X})(X+\bar{Y}) \cdot Z]'$

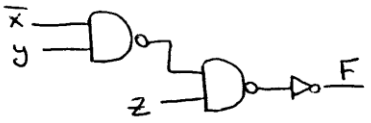
$g_5 = (g_3 \cdot Z)' = [(X+\bar{Y}) \cdot Z]'$

$F = (g_4 \cdot g_5)' = g_4 + g_5$

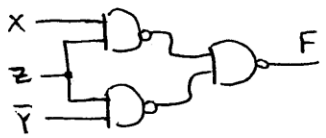
$= (X+\bar{Y}) \cdot Z + (X+\bar{Y})(Y+\bar{X})Z$

$= (X+\bar{Y}) \cdot Z$

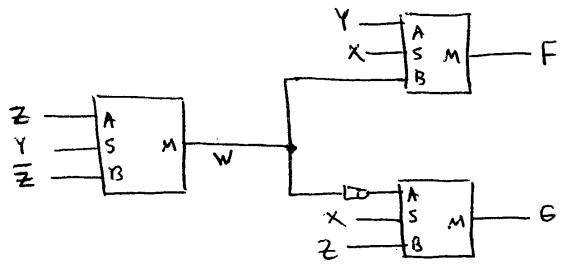
An equivalent circuit with fewer NAND gates:



OR



Q2



$W = \bar{Y}Z + Y\bar{Z}$

$F = \bar{X}Y + XW = \bar{X}Y + X\bar{Y}Z + XY\bar{Z}$

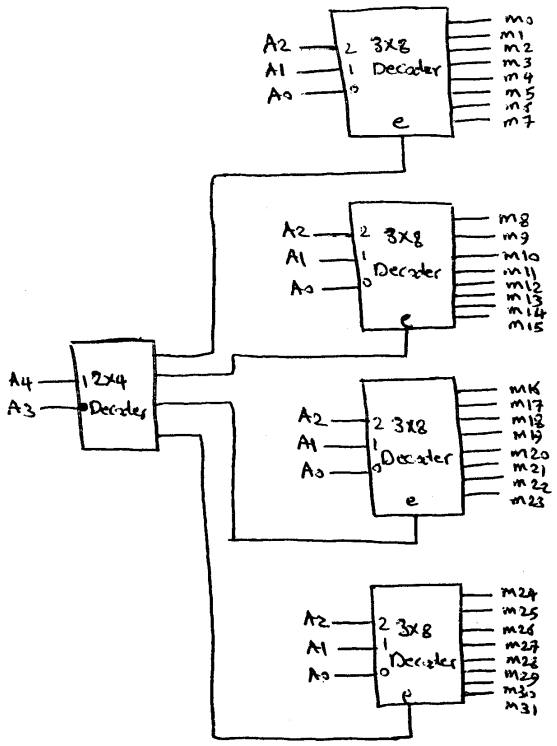
$G = \bar{X}\bar{W} + XZ = \bar{X}(\bar{Y}\bar{Z} + YZ) + XZ$

$= \bar{X}\bar{Y}\bar{Z} + \bar{X}YZ + XZ$

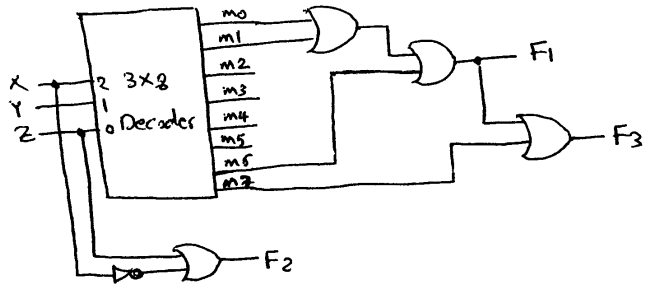
Q3

W	X	Y	Z	F	G
0	0	0	0	1	1
0	0	0	1	1	1
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	1	1
0	1	0	1	1	1
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	0	0
1	0	1	1	0	1
1	1	0	0	0	0
1	1	0	1	0	1
1	1	1	0	0	0
1	1	1	1	0	1

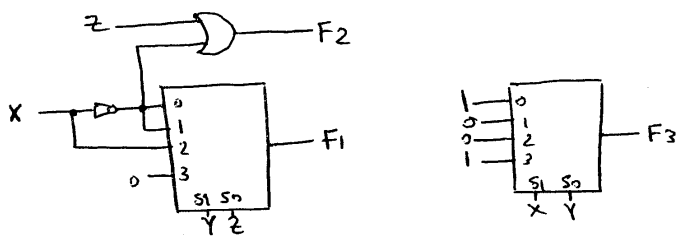
Q4



Q5 (i) $F_1 = \sum m(0,1,6)$, $F_3 = \sum m(0,1,6,7)$

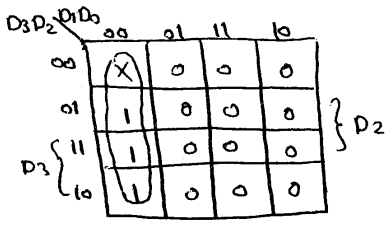


(22)

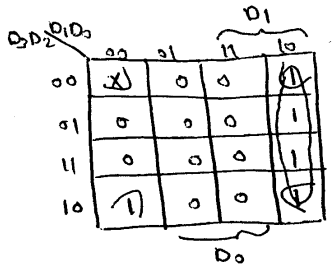


Q6

inputs				outputs		
D_3	D_2	D_1	D_0	A_1	A_0	V
X	X	X	1	0	0	1
X	X	1	0	0	1	1
X	1	0	0	1	0	1
1	0	0	0	1	1	1
0	0	0	0	X	X	0



$A_1 = \bar{D}_1 \bar{D}_0$

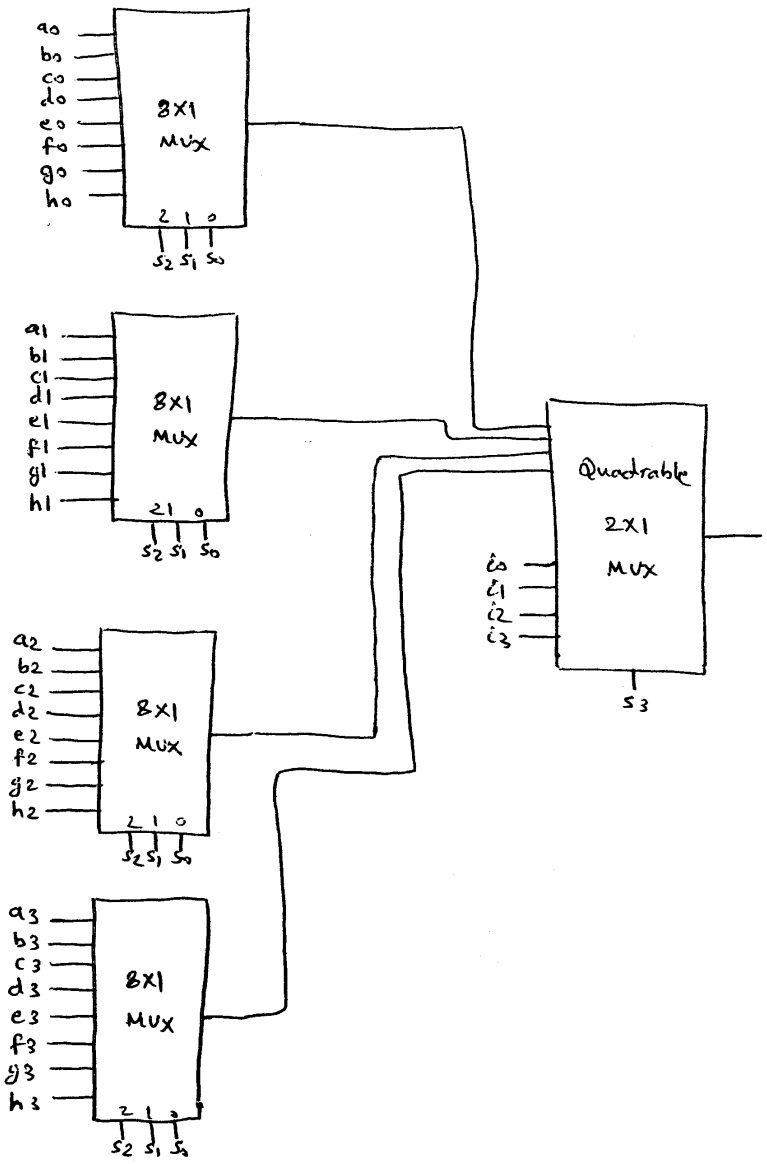


$A_0 = D_1 \bar{D}_0 + \bar{D}_2 \bar{D}_0$

$= \bar{D}_0 (D_1 + \bar{D}_2)$

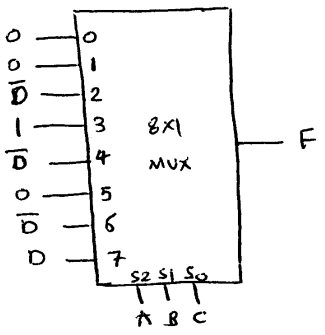
$V = D_0 + D_1 + D_2 + D_3$

Q7


a0
b0
c0
d0
e0
f0
g0
h0
8X1
MUX
2 1 0
S2 S1 S0
a1
b1
c1
d1
e1
f1
g1
h1
8X1
MUX
2 1 0
S2 S1 S0
a2
b2
c2
d2
e2
f2
g2
h2
8X1
MUX
2 1 0
S2 S1 S0
a3
b3
c3
d3
e3
f3
g3
h3
8X1
MUX
2 1 0
S2 S1 S0
Quadrable
2X1
MUX
i0
i1
i2
i3
S3

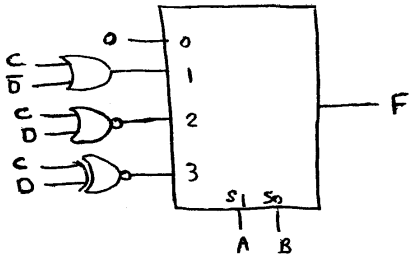
Q8 $F = \bar{A}B\bar{C}\bar{D} + \bar{A}BC\bar{D} + \bar{A}BCD + A\bar{B}\bar{C}\bar{D} + AB\bar{C}\bar{D} + ABCD$

(i)



(ii) $F = \bar{A}\bar{B}[0] + \bar{A}B[\bar{C}\bar{D} + C\bar{D} + CD] + A\bar{B}[\bar{C}\bar{D}] + AB[\bar{C}\bar{D} + CD]$

$= \bar{A}\bar{B}[0] + \bar{A}B[C + \bar{D}] + A\bar{B}[\bar{C}\bar{D}] + AB[\bar{C}\bar{D} + CD]$



Q9

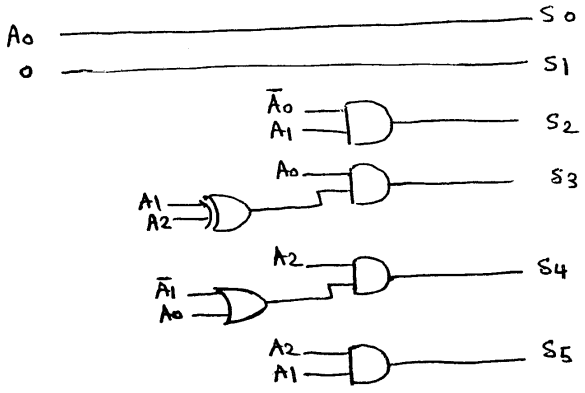
A_2	A_1	A_0	S_5	S_4	S_3	S_2	S_1	S_0
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1

$S_0 = A_0$, $S_1 = 0$, $S_2 = A_1 \bar{A}_0$, $S_3 = \bar{A}_2 A_1 A_0 + A_2 \bar{A}_1 A_0$

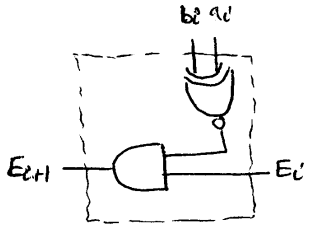
$\Rightarrow S_3 = A_0 [A_1 \oplus A_2]$

$S_4 = A_2 \bar{A}_1 + A_2 A_0 = A_2 [\bar{A}_1 + A_0]$

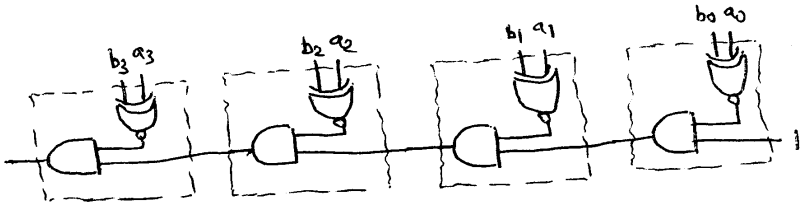
$S_5 = A_2 A_1$



Q10 The cell is designed as follows:



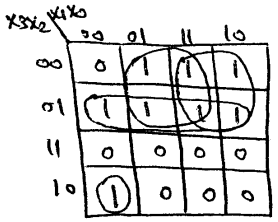
For example, a 4-bit equal comparator is shown below using this cell:



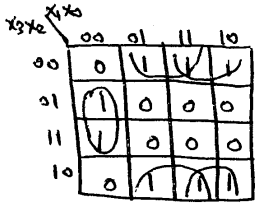
Q11

(a)

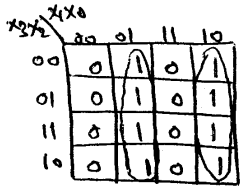
x_3	x_2	x_1	x_0	y_3	y_2	y_1	y_0
0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	0
0	0	1	1	1	1	0	1
0	1	0	0	1	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	0	1	1	0
1	0	1	1	0	1	0	1
1	1	0	0	0	1	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	0	1	0
1	1	1	1	0	0	0	1



$$Y_3 = x_3\bar{x}_2\bar{x}_1\bar{x}_0 + \bar{x}_3x_2 + \bar{x}_3x_1 + \bar{x}_3x_0$$
$$= x_3(x_2+x_1+x_0)' + \bar{x}_3(x_2+x_1+x_0)$$
$$= x_3 \oplus (x_2+x_1+x_0)$$



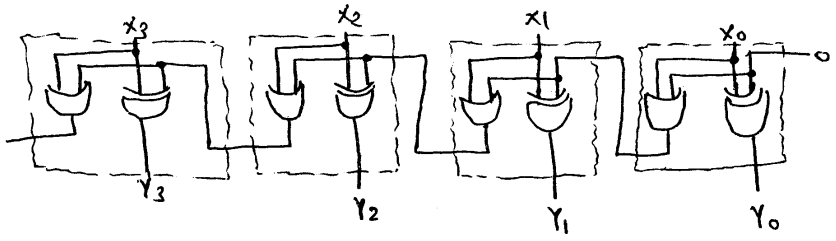
$$Y_2 = x_2\bar{x}_1\bar{x}_0 + \bar{x}_2x_1 + \bar{x}_2x_0$$
$$= x_2(x_1+x_0)' + \bar{x}_2(x_1+x_0)$$
$$= x_2 \oplus (x_1+x_0)$$



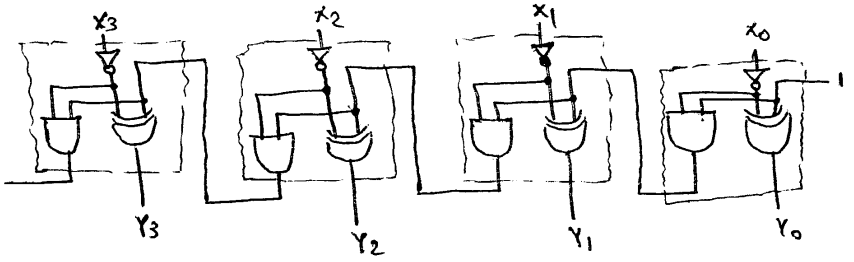
$$Y_1 = \bar{x}_1x_0 + x_1\bar{x}_0$$
$$= x_1 \oplus x_0$$

$$Y_0 = x_0$$

(b) As can be seen from the above equations, we have the following design:



Note that we can also get another solution based on finding the 1's complement and adding 1 to it as shown below:



Note also that this solution and the former are equivalent, i.e. one can be derived from the other, except for the last carry out. However, the last carry out is not part of the result.

(c) We will do this based on the first solution: