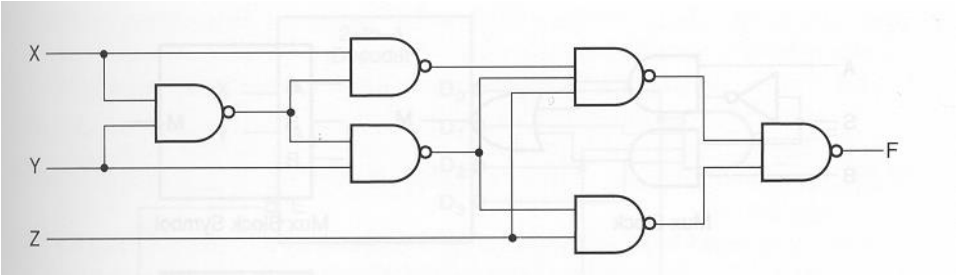
COE 202, Term 162

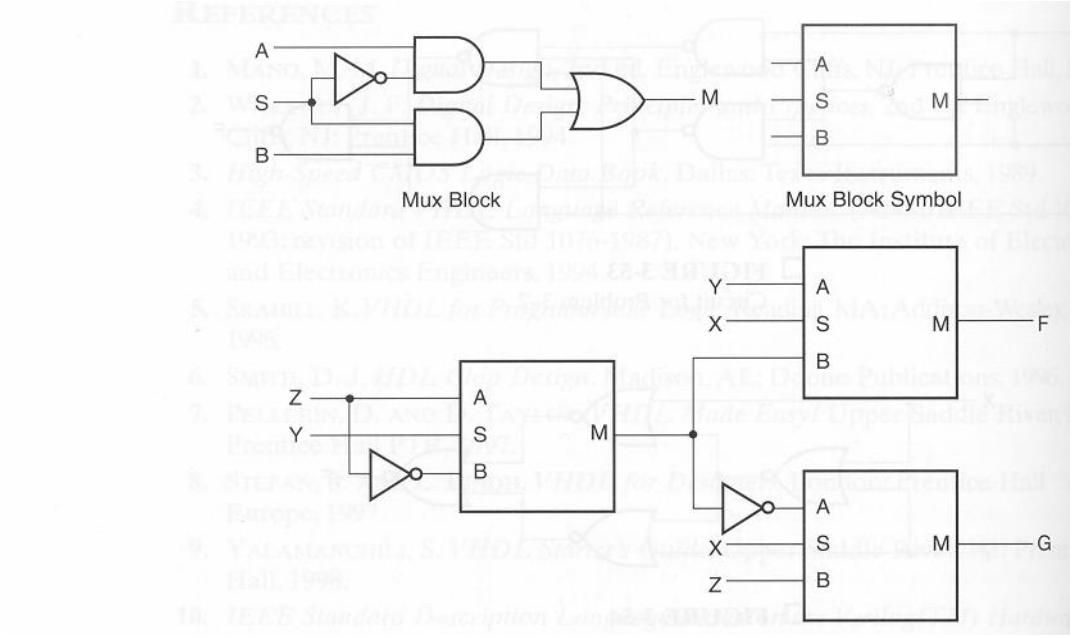
Digital Logic Design

HW# 5

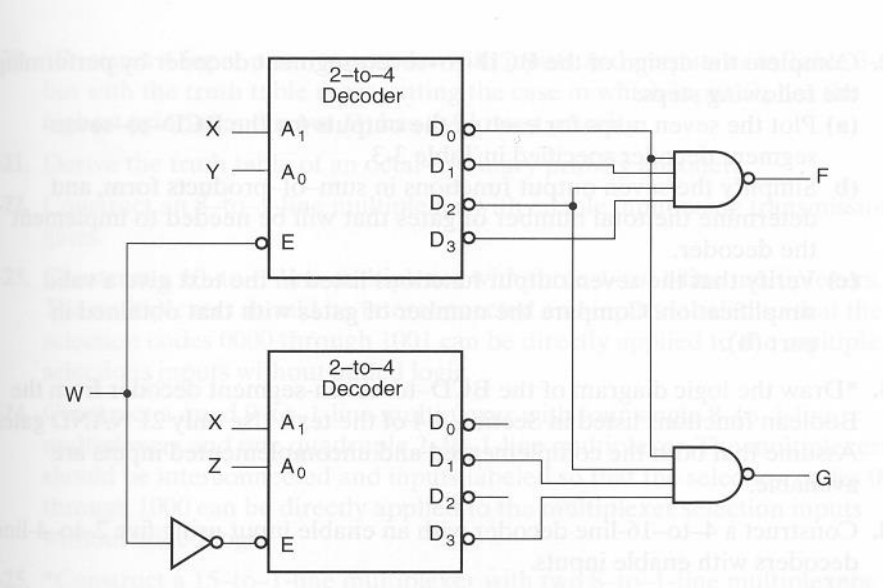
Q.1. Obtain the truth table for the circuit shown below. Draw an equivalent circuit for F with fewer NAND gates.



Q.2. Find simplified Boolean equations for the outputs F and G of the hierarchical circuit given below.



Q.3. Find the truth table for the outputs F and G of the hierarchical circuit shown below.



Q.4. Construct a 5-to-32 line decoder with four 3-to-8 line decoders with enable input and one 2-to-4 line decoder.

Q.5. A Combinational circuit is defined by the following three Boolean functions:

$F_1(X, Y, Z) = X`Y` + XYZ`$
$F_2(X, Y, Z) = X` + Z$
$F_3(X, Y, Z) = XY + X`Y`$

(i) Design the circuit with a 3x8 decoder, four 2-input OR gates, and an inverter.

(ii) Design the circuit with two 4x1 MUXs, one 2-input OR gate, and an inverter.

Q.6. Design a 4-input priority encoder with four inputs and three outputs including the valid bit but with the truth table representing the case in which input D_0 has the highest priority and input D_3 has the lowest priority.

Q.7. Construct a quad 9-to-1 line multiplexer with four single 8-to-1 line multiplexers and one quadruple 2-to-1 line multiplexer. The multiplexers should be interconnected and inputs labeled so that the selection codes 0000 through 1000 can be directly applied to the multiplexer selection inputs without added logic.

Q.8. Implement the following Boolean function F(A, B, C, D)=Σ m(4, 6, 7, 8, 12, 15) with:

(i) An 8x1 MUX. Assume that the inputs A, B, and C are used for the select lines.

(ii) A 4x1 MUX and external gates. Assume that the inputs A and B are used for the select lines.

Q.9. Design a Combinational circuit that accepts a 3-bit number and generates as output a binary number equal to the square of the input number.

Q.10. It is required to design a Combinational circuit that compares two n-bit numbers to see if they are equal or not. Design a circuit that has three inputs and one output, that can be used for each of the n bits, such that the circuit is connected in cascade by carry-like signals. One of the inputs to each cell is a carry input, and the single output is a carry output.

Q.11. Design three versions of the combinational circuit whose input is a 4-bit number and whose output is the 2's complement of the input number such that:

(i) The circuit is a simplified two-level circuit, plus inverters as needed for the input variables.

(ii) The circuit is made up of four identical two-input, two output cells, one for each bit. The cells are connected in cascade, with lines similar to a carry between them. The value applied to the rightmost carry bit is 0.

(iii) The circuit is redesigned with carry lookahead-like logic in order to speed up the circuit in part (ii) for use in larger circuits with 4n input bits.